1 Introduction

1.1 A technology in a hurry

Conventional wisdom indicates that it typically takes one to two decades before a materials-device breakthrough results in commercial products. Thus, since the first transparent thin-film transistors (TTFTs) were reported in 2003, conventional wisdom dictates that we will have to wait until between 2013 and 2023 to purchase transparent electronics-related merchandise.

We contend that transparent electronics is a technology-in-a-hurry and that there is no valid reason why product development should take so long. Given our perspective, this book constitutes a call-to-arms for the rapid acceleration of transparent electronics development towards commercialization. Furthermore this book can be construed as a prefatory transparent electronics roadmap, suggesting developmental directions to head and technological challenges to be met.

Two primary reasons why conventional wisdom is typically correct, so that product introduction usually does indeed require one or more decades to reach commercial maturity, involve the sequential nature of product development and the fact that early development is often conducted in academic environments which are isolated from industrial and commercial reality. Customarily, electronics product introduction follows a sequential development flow involving materials→ devices → product identification → circuits → systems → products. A more efficient approach would be to pursue all of these development topics concurrently, rather than sequentially, and in an industrially relevant context.

Thus, in order to attempt to foster a bit of industrial relevance, applications are discussed near the beginning of this book, inverting the natural topical sequential ordering somewhat. This may seem odd since transpar-

ent electronics 'killer apps' are admittedly either not yet well-defined or are presently unrealizable due to current limitations in transparent electronics or in a requisite auxiliary technology. However, this topical ordering inversion is meant to be intentionally provocative. Since transparent electronics is a nascent technology, we believe that its development will be most rapidly and efficiently accomplished if it is strongly application-driven, and if it is undertaken in a parallel fashion in which materials, devices, circuits, and system development are pursued concurrently. Hopefully, such a product-driven concurrent development strategy will lead to rapid technology assessment, the identification of new and most-likely unexpected applications, and an expeditious commercial deployment of this technology.

1.2 Pre-history

Two primary technologies which preceded and underlie transparent electronics are briefly overviewed. These topics are transparent conductive oxides (TCOs) and thin-film transistors (TFTs).

1.2.1 Transparent conducting oxides (TCOs)

TCOs constitute an unusual class of materials possessing two physical properties - high optical transparency and high electrical conductivity - that are generally considered to be mutually exclusive (Hartnagel et al. 1995). This peculiar combination of physical properties is only achievable if a material has a sufficiently large energy band gap so that it is non-absorbing or transparent to visible light, i.e., > ~3.1 eV, and also possesses a high enough concentration of electrical carriers, i.e., an electron or hole concentration > $\sim 10^{19}$ cm^{-3}, with a sufficiently large mobility, > ~1 cm^2 $V^{-1}s^{-1}$, that the material can be considered to be a 'good' conductor of electricity.

The three most common TCOs are indium oxide In_2O_3, tin oxide SnO_2, and zinc oxide ZnO, the basic electrical properties of which are summarized in Table 1.1. All three of these materials have band gaps above that required for transparency across the full visible spectrum.

Note that although the TCOs listed in Table 1.1 are considered to be 'good' conductors from the perspective of a semiconductor, they are actually very poor conductors compared to metals. For example, the conduc-

tivities of tungsten W, aluminum Al, and copper Cu, are approximately 100,000, 350,000, and 600,000 S cm^{-1}, indicating that the best In_2O_3 conductivity (for indium tin oxide or ITO) is about a factor of 10 to 60 lower than that of a typical integrated circuit contact metal. The low conductance of TCOs compared to metals has important consequences for both TCO and transparent electronics applications, some of which are explored in this book. The theoretical absolute limit of the conductivity for a TCO has been estimated to be 25,000 S cm^{-1} (Bellingham 1992).

Table 1.1. Electrical properties of common transparent conducting oxides (TCOs) Conductivities reported are for best-case polycrystalline films.

Material	Bandgap (eV)	Conductivity (S cm^{-1})	Electron concentration (cm^{-3})	Mobility (cm^2 V^{-1} s^{-1})
In_2O_3	3.75	10,000	$>10^{21}$	35
ZnO	3.35	8,000	$>10^{21}$	20
SnO_2	3.6	5,000	$>10^{20}$	15

Returning to Table 1.1, notice that all three of the TCOs included in this table are n-type, i.e., conductivity is a consequence of electron transport, and that the electron carrier concentration is strongly degenerate, i.e., the electron density exceeds that of the conduction effective band density of states by an appreciable amount (Pierret 1996; Sze and Ng 2007). All of the well-known and commercially relevant TCOs are n-type. p-type TCOs are a relatively new phenomenon and their conductivity performance is quite poor compared to that of n-type TCOs. To a large extent, the poor conductivity of p-type TCOs is due to the very low mobility of these materials, typically less than ~1 cm^2 $V^{-1}s^{-1}$, compared to mobilities in the range of ~10-40 cm^2 $V^{-1}s^{-1}$ for n-type TCOs.

The n-type mobilities indicated in Table 1.1 are quite small compared to those representative single crystal silicon materials and devices, which range from ~250-1,500 cm^2 $V^{-1}s^{-1}$. However, this mobility comparison between TCOs and single crystal silicon is a bit misleading since single crystal silicon mobility is not usually specified at doping concentrations as large as those typical of TCOs. In fact, it is reported that single crystal silicon mobility is independent of doping concentration above ~10^{19} cm^{-3}, with an electron mobility of ~90 cm^2 $V^{-1}s^{-1}$ and a hole mobility of ~50 cm^2 $V^{-1}s^{-1}$ (Baliga 1995). A low mobility at high carrier concentrations is, to a large extent, a consequence of intense ionized impurity scattering associated with high doping concentrations (Hartnagel et al.1995).

The first large-scale use of TCOs occurred during World War II, involving transparent heaters for de-icing applications in aircraft windshields (Ohring 1992). Since then, TCOs have been employed in a wide range of applications, including automobile, airplane, and marine widow defrosters; liquid-crystal, electrochromic, electroluminescent, and plasma displays; solar cell electrodes; infra-red reflectors for energy-efficient windows; transparent barrier layers for food, cigarette, and other types of packaging; heated glass freezer doors; heating stages for optical microscopes; photoconductors for television camera vidicons; electromagnetic shielding; touch screens; abrasion- and corrosion-resistant coatings; and gas sensors (Hartnagel et al. 1995; Ohring 1992; Ginley and Bright 1992; Hummel and Guenther 1995).

In these applications, TCOs are used electrically in a *passive* manner, as conductors or resistors. Typically, these types of applications require the TCO conductivity to be as large as possible for optimal performance. Thus, a great deal of research has been undertaken to maximize the TCO conductivity. This requires intentional doping of the TCO to extremely high concentrations. Commonly used TCO:n-type dopant combinations include In_2O_3:Sn, SnO_2:F, SnO_2:Sb, ZnO:F, and ZnO:Al. As evident from Table 1.1, substitutional doping at extremely high levels yields carrier concentrations in the range of 10^{20}-10^{21} cm^{-3}.

In contrast to conventional *passive electrical* TCO applications, the objective of transparent electronics is to use TCOs (or other types of TCs) in *active electronic* applications. In contradistinction to passive electrical TCO conductor applications, when used as a channel layer in a thin-film transistor, a TCO should have as low a carrier concentration as possible (thus, rendering it a transparent *non*-conducting oxide!). This is accomplished by avoiding the incorporation of n-type dopants, growing the TCO as fully oxidized as possible (since oxygen vacancies are well-known donors in most TCOs), and/or intentionally adding compensating dopants.

In conclusion, TCOs are basic constituents of transparent electronics. However, most TCO electrical applications require maximum conductivity, while transparent electronic applications depend upon rendering the TCO or TC, if the material is not an oxide, as resistive as possible, in the sense of having a low carrier concentration.

1.2.2 Thin-film transistors (TFTs)

The thin-film transistor (TFT) is another technology underlying transparent electronics, since it is the bridge between passive electrical and active electronic applications. Although TFTs were the subject of the earliest transistor patents (Lillienfield 1930; Lillienfield 1932; Lillienfield 1933; Heil 1935), the first actual realization of a TFT was reported in 1961 by Weimer and was fabricated via vacuum evaporation using CdS as a channel layer (Weimer 1961; Weimer 1962). Since TFTs are addressed in detail in Chapter 5, the remainder of this subsection is devoted to a brief discussion of early or peripheral attempts at fabrication of TFTs in which a TCO is used as the channel layer. None of these undertakings involved an attempt to realize a fully transparent TFT.

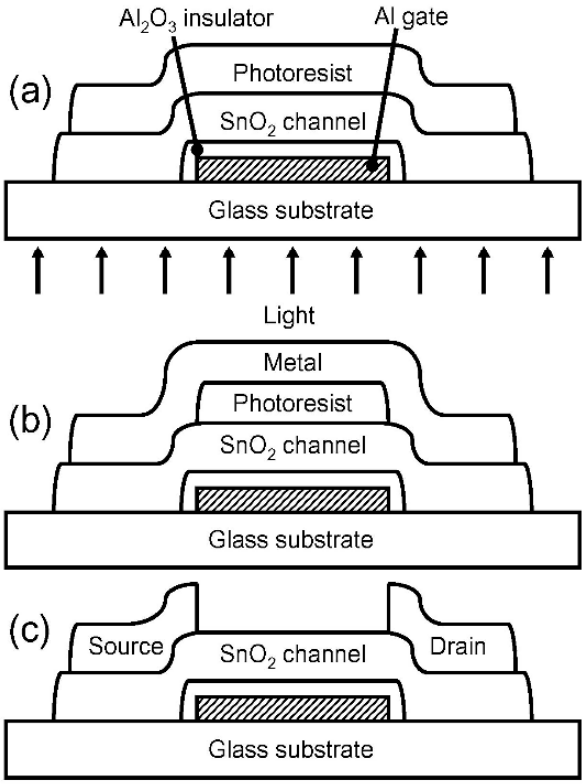

Fig. 1.1. Fabrication of a bottom-gate TFT with a SnO_2 channel layer. (a) Photoresist is patterned by bottom exposure, using the aluminum gate as a mask. (b) After photoresist development, a metal blanket coating is evaporated. (c) Final TFT device structure after lift-off (after Klasens and Koelmans 1964).

The first report of a TFT in which a TCO is used as a channel layer was in 1964, involving evaporated SnO_2 as the channel layer in a bottom-gate, staggered configuration (see Chapter 5 for a discussion of TFT device structures) on a glass substrate (Klasens and Koelmans 1964). The gate insulator is prepared by anodization of an evaporated and patterned bottom aluminum gate. A novel aspect of this paper pertains to a self-aligned lift-off process, illustrated in Fig. 1.1, in which photoresist covering the SnO_2 channel layer is patterned by bottom exposure, using the aluminum gate as a mask (Fig. 1.1a). Since SnO_2 is transparent, the photoresist which is not shielded by the aluminum gate is exposed. Subsequent development results in photoresist coverage only in aluminum gate shielded portions of the glass. Blanket deposition of an unspecified metal (Fig. 1.1b) and subsequent lift-off defines source-drain contacts (Fig. 1.1c). Thus, the very first report of a SnO_2 TFT makes use of the transparent nature of the SnO_2, yielding a novel processing methodology. Details regarding the electrical performance of this device are not provided in this short note, except that the transconductance is specified to be 0.13 mS mm^{-1} with a device gate length of 13 μm.

The first ZnO-based 'TFT' was announced in 1968 (Boesen and Jacobs 1968). The drain current-drain voltage performance of this device is marginal enough to warrant questioning whether or not this device can be accurately identified as a TFT, since the device does not saturate and it does not appear that the device can be turned off by application of a gate voltage of realistic magnitude. However, the drain current-drain voltage characteristics do exhibit negative curvature, suggesting that the drain voltage provides some of the negative feedback required for normal TFT operation, which is expected to exhibit pentode-like saturation, and also displays a small amount of gate voltage modulation of the drain current, albeit with some hysteresis. It is noteworthy that this device is fabricated using a lithium-doped single crystal of ZnO. Thus, these early researchers recognized that a TFT channel should have a very low carrier concentration, as achievable using lithium compensation doping. Evaporated SiO_x is used as the gate insulator and evaporated aluminum serves as the source, drain, and gate electrode material. The maximum transconductance observed is quoted as 1.1 mS mm^{-1} with a device gate length of 75 μm.

A more recent a report of a ZnO TFT was published in 2001 (Ohya et al. 2001). A bottom-gate TFT is fabricated on an oxidized silicon wafer using solution deposition of a 40 nm ZnO channel layer, starting with a zinc acetate precursor. The solution-deposited ZnO channel layer is then subjected to 600 ºC and 900 ºC anneals in air. Au electrodes are then evaporated

onto the ZnO channel layer, and serve as source & drain electrodes in a staggered configuration with respect to the silicon bottom-gate. In order for the device to function as a TFT, the second 900 ºC anneal is required to reduce the gate leakage current. Transmission electron microscopy and electron microprobe analysis reveal that this 900 ºC anneal leads to a reaction between ZnO and SiO_2, yielding an interfacial layer of Zn_2SiO_4 and ZnO. It is difficult to assess the TFT performance of this device since no drain current-drain voltage characteristics are provided. However, drain current-gate voltage transfer curves suggest that this device is operating in enhancement-mode with a very low mobility, ~10^{-3} cm^2 $V^{-1}s^{-1}$ as crudely estimated from the data provided in this paper.

The earliest SnO_2 'TFT' in which the drain current-drain voltage characteristics were actually reported exhibits even poorer performance than the initial ZnO 'TFT' discussed previously (Aoki and Sasakura 1970). The lack of saturation, inability to turn the device off, positive curvature of the drain current-drain voltage characteristics, and the almost negligible amount of gate voltage-induced drain current modulation strongly argues for more proper identification of this device as a voltage-controlled nonlinear resistor, rather than as a transistor. Very few details are provided regarding this device or its performance characteristics other than that the SnO_2 channel is deposited via vapor phase transport and subsequent oxidation; the device structure is coplanar with a top-gate using aluminum as the source, drain, and gate electrodes; and the gate insulator is a SiO-nitrocellulose double layer.

A ferroelectric 'transparent' TFT based on a SnO_2:Sb channel layer was reported in 1996 (Prins et al. 1996a,b). This device is fabricated on a $SrTiO_3$ substrate using pulsed laser deposition of a $SrRuO_3$ bottom gate electrode, a $PbZr_{0.2}Ti_{0.8}O_3$ ferroelectric gate insulator, and a SnO_2:Sb semiconductor layer. All of the layers are transparent except for the $SrRuO_3$ gate. Drain current-drain voltage and other conventional TFT electrical characteristics are not indicated for this device, nor for a similar ferroelectric memory device with an In_2O_3 channel layer (Seeger 1996), presumably because the primary purpose of this work is to demonstrate hysteresis of the drain current-gate voltage curve as evidence for a ferroelectric memory effect. These ferroelectric TFTs are distinctly different than the transparent TFTs discussed herein, since their SnO_2:Sb or In_2O_3 channel layers are intentionally doped to very high electron concentrations (>10^{18} cm^{-3}), whereas the channel layers of TFTs and TTFTs considered in this book are engineered to have as low a carrier concentration as possible. Differences between ferroelectric and 'normal' TFTs are a consequence of their differ-

ing applications involving, respectively, memory and general-purpose transistor functionality.

More recently, a SnO_2 TFT has been proposed as a novel gas sensor (Wöllenstein et al. 2003). This is motivated by the fact that SnO_2 is the most common material currently used in commercial conductive gas-sensors (Lantto 1992; Hozer 1994; Eranna et al. 2004; Batzill and Diebold 2005), and that a SnO_2 TFT offers the possibility of electronic control of the gas sensing sensitivity (Wöllenstein et al. 2003). In this sensor demonstration project, SnO_2 TFTs are fabricated on a silicon substrate covered with a 1 μm thick layer of SiO_2, using a bottom-gate, coplanar structure. Gate, source, and drain electrodes are formed using a Ta-Pt sandwich, the gate insulator is thermally evaporated SiO in an oxygen atmosphere, the SnO_2 channel is sputtered and is 60 nm thick, and the final device is rapid thermal annealed at 700 ºC for 60 minutes. The drain current-drain voltage characteristics of resulting SnO_2 TFTs are quite poor; exhibiting severe drooping in the 'saturation' region at large gate voltages, indicative of either gate leakage or pronounced channel/interface electron trapping, and the TFT does not appear to turn off with application of gate biases of reasonable magnitude. However, evidence is provided that this SnO_2 TFT behaves as a gas sensor and that its sensitivity may be adjusted, at least to some extent, via application of a gate voltage.

1.3 The stage is now set

Now that TCOs and TFTs - the two technologies underlying transparent electronics - have been briefly overviewed, it is appropriate to review previous work that has been reported to date related to the early development of transparent electronics. This is accomplished in Chapter 2.

2 A Review of Prior Work

2.1 Origins

The 'birth' of transparent electronics can arguably be dated to the first report of a highly conductive p-type transparent oxide $CuAlO_2$ (Kawazoe et al. 1997).

In the same issue of *Nature* in which $CuAlO_2$ is reported, the implications of this achievement are highlighted in a perspective article which discusses 'invisible circuits' (Thomas 1997). It is asserted that invisible electronic circuits will lead to new applications, significantly beyond those involving passive TCOs.

In retrospect, it is somewhat ironic that the announcement of a p-type TCO would precipitate the genesis of transparent electronics. The availability of p-type TCOs is indeed required for the realization of *bipolar* transparent electronics. However, almost all of the progress to date in transparent electronics involves the exclusive utilization of *unipolar,* n-type devices. This is not to disparage the importance of obtaining p-type TCOs with better electrical performance since this is critical for future n- and p- complementary TTFT applications and transparent optical sources. Rather, it is a bit paradoxical that a bipolar breakthrough would stimulate innovation in the unipolar arena.

Returning to $CuAlO_2$, attractive attributes of pulsed laser deposited polycrystalline thin films of this material include a Hall mobility in excess of 10 $cm^2\ V^{-1}s^{-1}$ and a hole carrier concentration of $\sim 10^{17}\ cm^{-3}$, leading to a conductivity of ~1 S/cm (Kawazoe et al.1997). Although this conductivity is about 10,000 times smaller than the best ITO n-type TCO, the p-type carrier concentration of this unintentionally doped TCO is three to four orders of magnitude lower than that typical of doped n-TCOs, suggesting that intentionally doped p-TCOs may eventually be engineered to be con-

ductive enough for practical, high-conductivity applications. The direct bandgap of $CuAlO_2$ is reported to be 3.5 eV, which is ideally suited for fully-transparent TCO applications.

Table 2.1 summarizes p-type TCO and TC development efforts that have been reported to date. Since the main thrust of this section is to present an overview of transparent electronics, only a few brief comments related to this table are offered here; a more comprehensive discussion of p-type TCOs and TCs is included in Chapter 3. The development of p-TCOs has recently been reviewed (Banerjee and Chattopadhyay 2005, Sheng et al. 2006).

Table 2.1. Selected properties of p-type transparent conducting oxides (TCOs) and transparent conductors (TCs). [Transparency assessment: Excellent > ~70%, Fair > ~30%, and Poor < ~30% across the visible portion of the electromagnetic spectrum for a thin film thickness of ~200 nm. The energy band gap, E_G, of the material is specified if it is lower than that required for full transparency across the entire visible spectrum.]

Material	Conductivity ($S\ cm^{-1}$)	Mobility ($cm^2\ V^{-1}s^{-1}$)	Transparency	Reference
NiO	7	~2	Fair	Sato et al. 1993
	0.14		Fair	Ohta et al. 2003
$AlCuO_2$	1	10.4	Excellent	Kawazoe et al. 1997
	0.3	0.13		Yagani et al. 2000
$SrCu_2O_2$:K	0.048	0.46	Excellent	Kudo et al. 1998 , Ohta et al. 2002
In_2O_3-Ag_2O	100	17	Poor	Minami et al. 1998
LaCuOS:Sr	0.026		Excellent	Ueda et al. 2000
$CuInO_2$:Ca	0.0028		Excellent	Yanagi et al. 2000
$CuScO_2$:O	30	<0.5	Poor	Duan et al. 2000
	25		Poor	Kykyneshi et al. 2004
$CuScO_2$:Mg	0.01		Excellent	Kykyneshi et al. 2004

Table 2.1 (continued).

Material	Conductivity ($S\ cm^{-1}$)	Mobility ($cm^2\ V^{-1}s^{-1}$)	Transparency	Reference
$CuGaO_2$	0.063	0.23	Excellent	Ueda et al. 2001
$CuYO_2$:Ca	0.3 -1	<0.5	Fair	Jayaraj et al. 2001
$CuCrO_2$:Mg	220	<0.5	Poor	Nagarajan et al. 2001a
$AgMO_2$ (M = Sc, In, Cr, Ga)	<0.01			Nagarajan et al. 2001b
$AgCoO_2$	0.2		Fair	Tate et al. 2002
$CuGaO_2$:Fe	~1		Fair	Tate et al. 2002
$Sr_2Cu_2ZnO_2S_2$: Na	0.12		E_G = 2.6 eV	Hirose et al. 2002
$BaCu_2S_2$	17	3.5	E_G = ~2.3 eV	Park et al. 2002
$CuNi_{0.67}Sb_{0.33}O_2$:Sn	0.05		Fair	Nagarajan et al. 2002
LaCuOSe	24	8	E_G = 2.8 eV	Hiramatsu et al. 2003
LaCuOSe:Mg	140	4	E_G = 2.8 eV	Hiramatsu et al. 2003
BaCuSeF:K	43 (pellets)			Yanagi et al. 2003b, Yanagi et al. 2006
BaCuSF:K	82 (pellets)			Yanagi et al. 2003b
	100 (pellets) 1 (films)			Yanagi et al. 2003a, Yanagi et al. 2006
$ZnRh_2O_4$	0.7		$E_G \approx 2.1$ eV	Mizoguchi et al. 2003
$La_2CdO_2Se_2$				Ueda et al. 2006
$La_2SnO_2Se_3$				Ueda et al. 2006

As evident from Table 2.1, a number of materials have been investigated for p-type transparent electronics applications. Almost all of the references included in this table are of a very recent date, and are motivated to a large extent by Kawazoe et al.'s 1997 $AlCuO_2$ paper. The initial exploratory development of many of these materials was accomplished prior to the references included in this table, as reviewed by Banerjee and Chattopadhyay 2005 and Sheng et al. 2006. A majority of the materials included in Table 2.1 are oxides, although several types of non-oxide based p-type materials are also listed, i.e., oxysulfides, oxyselenides, sulfide-fluorides, and selenide-fluorides. If a material included in Table 2.1 is not followed by a colon, this indicates that the p-type character of the material is a consequence of native defects, usually either cation vacancies or anion interstitials. A colon after a material chemical formula means that the material is intentionally doped, either substitutionally on the cation site or by interstitial intercalation if an oxygen anion is the dopant. Note that not all of the materials included in Table 2.1 have energy band gaps large enough to obtain full transparency across the entire visible portion of the electromagnetic spectrum, i.e., $E_G \geq 3.1$ eV. GaN and especially ZnO are noticable omissions from Table 2.1.

It is clear from Table 2.1 that obtaining high conductivity and transparency from a p-type material is a challenging task. Typically, the hole mobility for a wide band gap material is very low, less than ~1 $cm^2\ V^{-1}s^{-1}$, which necessitates having a large hole concentration in order to obtain a high conductivity. There is often a trade-off between conductivity and transparency. For example, unintentionally doped $CuScO_2$ films are highly insulating and transparent, whereas oxygen intercalation greatly increases their conductivity and concomitantly degrades their transparency (Tate et al. 2002; Kykyneshi et al. 2004).

From a transparent electronics perspective, the most important p-type TCO development prior to 2003 is arguably the demonstration of a transparent pn heterojunction ultraviolet (UV) light-emitting diode (Ohta et al. 2000). This device is constructed using p-$SrCu_2O_2$ and n-ZnO layers, both grown epitaxially via pulsed laser deposition (PLD). Sharp electroluminescence peaking at 382 nm is observed at ~3 V above the forward bias threshold, and is attributed to exciton-exciton collusion or electron-hole plasma recombination within the ZnO layer. This transparent UV light-emitting diode demonstration is considered to be exceedingly important since a notable transparent electronics 'killer app' is a transparent display.

This demonstration by Ohta et al. constitutes a first step towards the realization of a light-emitter for an inorganic transparent display.

2.1.1 Transparent electronics - 2003

Transparent electronics development took off in earnest in early 2003 with the contemporaneous report of a ZnO TFT or TTFT by three groups (Masuda et al. 2003; Hoffman et al. 2003; Carcia et al. 2003).

Masuda et al. used PLD at a substrate temperature of 450 ºC under an oxygen atmosphere to deposit a low carrier concentration (<5 X 10^{16} cm^{-3}) ZnO channel layer for the realization of a bottom-gate TTFT, as well as several other types of bottom-gate non-transparent TFTs using silicon substrates (Masuda et al. 2003). The TTFT is constructed on a glass substrate using ITO as the gate contact, a two-layer SiO_2-SiN_x gate insulator deposited by plasma-enhanced chemical vapor deposition, a 250 nm thick ZnO channel layer, and IZO source-drain electrodes (presumably indium zinc oxide, although this is not specified in the paper). The dual layer gate dielectric features SiN_x next to the ZnO channel layer. The dual layer gate is used to suppress insulator leakage that is found to occur when a single SiO_2 layer is used. The TTFT has a transmittance of more than 80% in the visible portion of the electromagnetic spectrum. The TTFT electrical performance is rather poor compared to the other non-transparent TFTs fabricated on silicon substrates; it operates in depletion-mode, does not exhibit full saturation, and does not appear to fully turn off under the application of a depleting gate voltage. In contrast, silicon substrate TFTs operate in either enhancement- or depletion-mode (depending on the channel layer carrier concentration), exhibit hard saturation, and near-ideal transistor drain current-drain voltage characteristics. The field-effect mobility of the non-transparent TFT is 0.031 and 0.97 cm^2 $V^{-1}s^{-1}$ for the enhancement- and depletion-mode device, respectively, and the Hall mobility of a ZnO thin film is found to be 0.7 cm^2 $V^{-1}s^{-1}$. The drain current on-to-off ratio for the ZnO TFTs on silicon substrates is 10^5. One reason for the poorer performance of the TTFT compared to the non-transparent TFT is associated with the insulator surface roughness, which is found via atomic force microscopy analysis to be R_{rms} = 5.591 nm and 0.157 nm for the glass and silicon substrate TFT, respectively.

Hoffman et al. used ion beam sputtering to deposit 100 nm thick ZnO channel layers for their TTFTs (Hoffman et al. 2003). They also employed a staggered, bottom-gate TTFT device structure, using ITO as the gate,

source, and drain electrodes, and aluminum-titanium oxide (ATO) deposited by atomic layer epitaxy as the gate dielectric. Two post-deposition anneals are used. A 600-800 ºC rapid thermal anneal (RTA) in oxygen is used after deposition of the ZnO channel layer to improve crystallinity, and a 300 ºC RTA is performed to improve the transparency of the ITO layer. These TTFTs have an optical transmission (including the substrate) of ~75% in the visible portion of the electromagnetic spectrum. Drain current-drain voltage characteristics indicate that these devices operate in enhancement-mode with threshold voltages of ~10-20 V, but drain current-gate voltage transfer characteristics plotted on a logarithmic scale clarify that a gate voltage of ~-10 V is required to completely turn off the device (this voltage is denoted as the turn-on, V_{ON}, in contradistinction to the threshold voltage, V_T; see Chapter 5 for a more complete discussion). Field-effect mobilities are found to range from ~0.3-2.5 $cm^2\ V^{-1}s^{-1}$ and the drain current on-to-off ratio is reported to be ~10^7.

Carcia et al. used rf magnetron sputtering at near room temperature to deposit ZnO in order to fabricate ZnO TFTs on silicon substrates (Carcia et al. 2003). The most significant aspect of this work is a demonstration of low-temperature processing, which implies that ZnO TFTs are potentially useful for flexible electronics applications using temperature-sensitive substrates. A staggered, bottom-gate TFT device structure is once again used, with heavily-doped silicon with a 100 nm thick thermal oxide functioning as the gate contact-insulator, and Ti-Au serving as the source and drain electrodes. Even though the ZnO is deposited at near room temperature, i.e., with no intentional substrate heating, the electrical performance of these ZnO TFTs is quite good. The best devices exhibit ideal drain current-drain voltage characteristics, field-effect mobilities >2 $cm^2\ V^{-1}s^{-1}$, and drain current on-to-off ratios of >10^6.

A few months after the appearance of Masuda et al., Hoffman et al., and Carcia et al.'s papers, Nishii et al. reported the fabrication of a ZnO TFT with an improved field-effect mobility of as high as 7 $cm^2\ V^{-1}s^{-1}$ at a maximum process temperature of 300 ºC (Nishii et al. 2003). Additionally, they obtain a channel mobility of ~2 $cm^2\ V^{-1}s^{-1}$ at a maximum process temperature of 150 ºC, thus showing process compatibility with polymer substrates. The ZnO channel layer and the $CaHfO_x$ gate buffer layer insulator are both deposited by PLD. Silicon nitride is used as the gate insulator. The TFT device structure, dimensions, materials, and maximum processing temperature are identical to those used in commercial amorphous silicon (a-Si) TFTs in active-matrix liquid-crystal displays (AMLCDs), except for the $CaHfO_x$ gate buffer layer and the ZnO channel layer. There-

fore, Nishii et al.'s work indicates that ZnO TTFTs with improved performance can be readily integrated into AMLCDs as a replacement for a-Si switching transistors.

Very shortly after these first four ZnO TTFT papers were published, Nomura et al. reported the fabrication of a single crystal TTFT with an extraordinarily large field-effect mobility of ~80 cm^2 $V^{-1}s^{-1}$ (Nomura et al. 2003). Unlike the ZnO TTFTs described previously, the device structure employed is coplanar with a top-gate. To accomplish epitaxial growth of the 120 nm thick $InGaO_3(ZnO)_5$ channel layer, a yttria-stabilized zirconia substrate is used. The $InGaO_3(ZnO)_5$ channel layer is noteworthy since it is a superlattice consisting of alternating stacked layers of InO_2^- and $GaO(ZnO)_5^+$ blocks. It is grown at 700 ºC by PLD, followed by a thermal anneal at 1400 ºC. HfO_2 is used as the top-gate insulator and ITO serves as the source, drain, and gate contact. The HfO_2 and ITO layers are formed by PLD. The performance of this TTFT is in most respects excellent: optical transmittance >80%, enhancement-mode operation with $V_T \approx$ 3 V & $V_{ON} \approx$ -0.5 V, drain current on-to-off ratio of ~10^6, and negligible photoresponse. The drain current-drain voltage characteristics reported possess a slight droop in the saturation regime, probably due to a small amount of carrier trapping at the HfO_2-$InGaO_3(ZnO)_5$ interface or, less likely, in the channel. The excellent mobility obtained with this device is likely due to the fact that the uppermost interfacial transport layer is InO_2^-. Another reason for the excellent performance of this device is attributable to the very high resistivity of the channel layer, ~10^{-5} S cm^{-1}, and its very low carrier concentration, ~10^{13} cm^{-3}.

Subsequent to the appearance of these earliest TTFT-related publications, there were in 2003 three other reports involving the fabrication and modeling of ZnO TTFTs or related TFTs (Norris et al. 2003; Hossain et al. 2003; Bae et al. 2003).

Norris et al. fabricated a ZnO TTFT with a channel layer formed via spin coating using a zinc nitrate precursor solution which is converted to ZnO by baking in air at 600 ºC, followed by a 700 ºC RTA in oxygen (Norris et al. 2003). The most notable aspect of this work is that spin-coating deposition offers a simple, low-cost processing alternative to vacuum processing. The mobility performance of this staggered, bottom-gate TTFT is not as good as that reported previously via ion beam sputtering (Hoffman et al. 2003), with a maximum channel mobility of 0.20 cm^2 $V^{-1}s^{-1}$. Also, these devices have more light sensitivity than those prepared by sputtering. However, these spin-coated ZnO TTFTs exhibit true enhance-

ment-mode characteristics with positive V_{ON}'s and $V_T \approx$ 10-20 V. Additionally, these devices are highly transparent and possess a drain current on-to-off ratio of nearly 10^7.

Hossain et al. performed the first two-dimensional device simulations of ZnO TTFTs, assuming that the polycrystalline nature of the ZnO is primarily responsible for its performance (Hossain et al. 2003). The ZnO channel is assumed to have a variable density of uniformly sized, vertically-oriented, rectangular grains. Each grain is modeled as a back-to-back Schottky barrier with a Gaussian density of deep levels localized at grain boundaries. Electron transport is assumed to occur by drift-diffusion or thermionic emission. Within the context of their model, three properties of the polycrystalline ZnO thin film control the TFT performance: the grain size, the electron concentration within each grain, and the density of grain boundary traps. These simulations indicate that there are two primary effects associated with having a dense grain boundary density, as expected for low-temperature processed ZnO with grain sizes ranging from about 50-100 nm. First, a high channel resistivity is obtained due to space charge region merging between grains; this is desirable, since it will lead to enhancement-mode transistor behavior. Second, the channel mobility is dramatically degraded by energy barriers and trapping associated with grain boundaries; this is undesirable since it decreases the current drive capability of a transistor.

Bae et al. constructed a bottom-gate, staggered ZnO TFT and explored its utility as a novel UV photodetector (Bae et al. 2003). A thermal silicon oxide on a silicon substrate is used as the bottom gate, a 100 nm thick ZnO channel is deposited via rf magnetron sputtering, and Al source/drain electrodes are thermally evaporated. A 350 ºC post-deposition RTA in forming gas (H_2:N_2 = 1:10) is used to increase the conductance of the ZnO channel and to reduce the contact resistance of the Al contacts. A subsequent investigation indicates that H-annealing shifts the threshold to more negative voltages and increases the channel mobility, presumably due to the incorporation of H or introduction of oxygen vacancies, both of which are shallow donors in ZnO (Bae et al. 2004). Dark TFT performance parameters include $V_T \approx 3$ V, $V_{ON} \approx -25$ V, $\mu_{SAT} \approx 0.1$ cm^2 V^{-1}s^{-1}, drain current on-to-off ratio $\approx 10^6$, and subthreshold swing ≈ 4.5 V/decade. This ZnO TFT is confirmed to function as a UV detector, exhibiting about an order of magnitude more photocurrent than dark current at a gate voltage of 40 V. However, the UV discrimination of this device with respect to visible light is non-ideal, with blue, green, and red light yielding progressively less photosensitivity.

2.1.2 Transparent electronics - 2004

Five transparent electronics reports of significance appeared in 2004 (Kwon et al. 4004; Hoffman 2004; Fortunato et al. 2004a,b; Presley et al. 2004; Nomura et al. 2004).

Kwon et al. point out that a primary challenge facing TTFT development is to minimize the carrier concentration in the active channel (Kwon et al. 2004). Their approach to accomplish this objective is to employ phosphorous-doped $Zn_{0.9}Mg_{0.1}O$ as the channel layer. This strategy suppresses the channel electron concentration in two ways. First, alloying of ZnO with Mg increases the band gap, which apparently leads to a reduction in the donor density or an increase in the donor activation energy. Second, phosphorous substitution onto the oxygen site introduces an acceptor level, thereby compensating donors present in the channel. PLD is utilized to form the 50 nm $Zn_{0.9}Mg_{0.1}O$:P channel layer, rf magnetron sputtering is used to deposit a 100 nm HfO_2 insulator in a top-gate configuration, and ITO serves as the top gate contact and bottom source/drain contacts in a staggered device structure. The performance of their TFT is dominated by a large amount of gate leakage, rendering questionable their conclusions related to electrical assessment of this device. They assert that their device operates in enhancement-mode and possesses a field-effect mobility of 5.32 $cm^2\ V^{-1}s^{-1}$, but it is impossible to unambiguously estimate threshold voltages when a TFT has a large leakage current and to extract a field-effect mobility from a device which has a negative differential transconductance in the regime where this extraction is performed.

Hoffman's paper is very important in the history of transparent electronics because he introduces a new, physically-based methodology for channel mobility assessment and he also provides experimental data clarifying mobility-gate voltage trends for ZnO TFTs (Hoffman 2004).

With regard to mobility assessment, two different types of channel mobility are physically deduced, as a function of gate voltage. The average mobility as a function of gate voltage, $\mu_{AVG}(V_{GS})$ physically corresponds to the *average* mobility of *all* of the carriers present in the channel, is calculated from the measured channel conductance (g_d) in a fashion which is similar to how the more well-known effective mobility, μ_{EFF}, is calculated (Schroder 2006), and is the best channel mobility figure-of-merit for predicting the circuit performance potential of a TFT. (Hong et al. 2007) In contrast, the incremental mobility as a function of gate voltage, $\mu_{INC}(V_{GS})$, physically corresponds to the *incremental* mobility of carriers *added* to the

channel as the gate voltage differentially increases in magnitude, is calculated from the measured *differential* channel conductance ($\partial g_d/\partial V_{GS}$) in a fashion similar to that of how the more well-known field-effect mobility, μ_{FE}, is calculated (Schroder 2006), and is the best mobility figure-of-merit for assessing the physics of carrier transport in a TFT (see Chapter 5 for a more complete treatment of channel mobility). Table 2.2 is a comparison between conventional channel mobilities and those introduced by Hoffman. Note that μ_{FE} and μ_{INC} are identical except that the transconductance divided by V_{DS} portion of μ_{FE} is replaced by the differential channel conductance in μ_{INC}. Similarly, μ_{EFF} and μ_{AVG} are identical except that V_T in μ_{FE} is replaced by V_{ON} in μ_{AVG}. A remarkable aspect of this paper is that although field-effect transistor channel mobility assessment has been extensively undertaken for more than 40 years in the context of effective and field-effect mobilities, this paper appears to offer the first physical interpretation of channel mobilities.

Table 2.2. A comparison between conventional channel mobilities i.e., field-effect, μ_{FE}, & effective, μ_{EFF}, and physically-based channel mobilities introduced by Hoffman 2004, i.e., incremental, μ_{INC}, & average, μ_{AVG} (see Chapter 5 for a more detailed discussion of mobility).

Conventional channel mobility	**Physically-based channel mobility**
$\mu_{FE}(V_{GS}) = \underset{V_{DS}\to 0}{Lim}\left[\dfrac{g_m(V_{GS})}{\dfrac{W}{L}C_G V_{DS}}\right]$	$\mu_{INC}(V_{GS}) = \underset{V_{DS}\to 0}{Lim}\left[\dfrac{\dfrac{\partial g_d(V_{GS})}{\partial V_{GS}}}{\dfrac{W}{L}C_G}\right]$
$\mu_{EFF}(V_{GS}) = \underset{V_{DS}\to 0}{Lim}\left[\dfrac{g_d(V_{GS})}{\dfrac{W}{L}C_G(V_{GS}-V_T)}\right]$	$\mu_{AVG}(V_{GS}) = \underset{V_{DS}\to 0}{Lim}\left[\dfrac{g_d(V_{GS})}{\dfrac{W}{L}C_G(V_{GS}-V_{ON})}\right]$

W = channel width, L = channel length, C_G = gate capacitance per unit area, V_{DS} = drain-source voltage, V_{GS} = gate-source voltage, V_T = threshold voltage, V_{ON} = turn-on voltage, g_d = drain conductance = $\partial I_D/\partial V_{DS}$, g_m = transconductance = $\partial I_D/\partial V_{GS}$. The limit of V_{DS} approaching zero ensures that the transistor is in the linear regime of device operation.

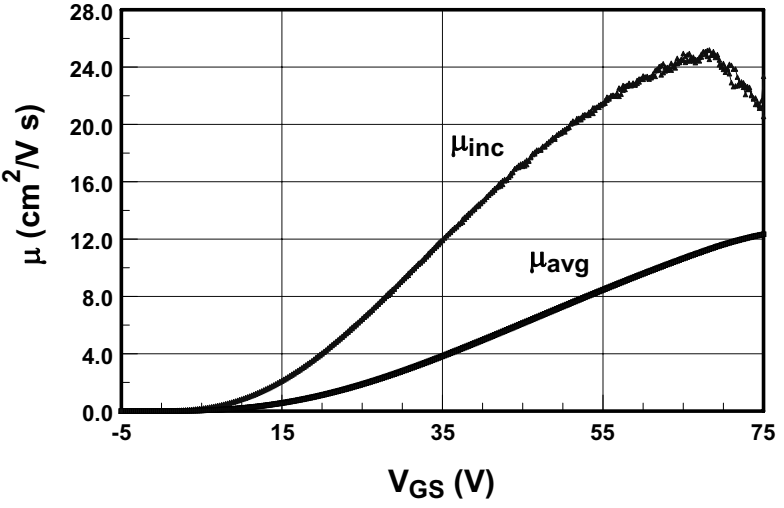

Fig. 2.1. Extracted incremental and average mobilities, μ_{INC} and μ_{AVG}, as obtained from experimental I_D-V_{GS} data from a ZnO TFT. Reused with permission from R. L. Hoffman, Journal of Applied Physics, 95, 5813 (2004). Copyright 2004, American Institute of Physics.

Finally concluding this discussion of Hoffman's paper, Fig. 2.1 illustrates the extracted mobilities $\mu_{INC}(V_{GS})$ and $\mu_{AVG}(V_{GS})$ for a ZnO TFT with a thermal silicon oxide serving as the bottom-gate insulator. Beginning at $V_{ON} \approx -4$ V, μ_{inc} increases with increasing V_{GS}. μ_{INC} is initially low just beyond V_{ON} since most of the initially injected channel electrons are trapped at interface states and/or channel layer traps. As V_{GS} increases, these traps become filled so that a smaller and smaller fraction of the incrementally added carriers to the channel are trapped. At approximately $V_{GS} = 65$ V, μ_{INC} peaks and subsequently decreases, most likely due to a complete filling of traps so that interfacial roughness scattering dominates for V_{GS} greater than 65 V, reducing the mobility as electrons are localized closer to the interface and experience more intense scattering. Thus, the $\mu_{INC}(V_{GS})$ trend is directly correlated to the channel electron transport physics, dominated first by trapping and then by interface scattering. In contrast, the $\mu_{AVG}(V_{GS})$ trend simply represents a moving average of μ_{INC}, evaluated from V_{ON} to V_{GS}. For TFTs, μ_{AVG} is usually smaller than μ_{INC}

since carrier trapping typically dominates and μ_{AVG} corresponds to the average mobility of all of the carriers in the channel, including those which are not contributing to the drain current but are immobilized in traps. However, for MOSFETs, μ_{INC} is usually smaller than μ_{AVG} (Schroder 2006). This appears to be a consequence of the fact that carrier trapping is of negligible importance in MOSFETs but, rather, that interface scattering dominates.

Returning once more to Fig. 2.1, notice that rather large maximum mobilities of μ_{INC} = 25 $cm^2\ V^{-1}s^{-1}$ and μ_{AVG} =12 $cm^2\ V^{-1}s^{-1}$ are obtained, but that reaching these maximum values requires the application of extremely large gate voltages, approximately 70 V and 80 V above V_{ON}. There are several important consequences of this result. First, different types of mobilities lead to different quantitative estimates of the channel mobility. Second, the magnitude of the channel mobility is a function of the gate voltage. Third, although maximum mobility is an important figure-of-merit for assessing the performance of a TFT, for practical applications it is also critical to be able to reach this maximum mobility at a minimal gate overvoltage, i.e., the applied gate voltage minus the turn-on voltage. Fourth, a sluggish mobility trend with respect to V_{GS}, such as that shown in Fig. 2.1, appears to be associated with carrier trapping, very likely grain boundary-related trapping for ZnO TFTs, as discussed by Hossain et al. 2003. Optimal TFT and TTFT device performance will depend strongly on trap tailoring such that enhancement-mode device behavior is obtained and yet high maximum mobilities are reached at small gate overvoltages.

Fortunato et al. report the first ZnO TTFT in which the entire device is fabricated at near-room temperature, i.e., with no intentional heating of the substrate (Fortunato et al. 2004a). Their device is a staggered, bottom-gate TTFT in which ITO is used as the bottom gate contact, the insulator is a 200 nm silicon oxynitride and the channel layer is 150 nm of ZnO, both deposited by rf magnetron sputtering, and the top drain/source electrodes are ZnO:Ga.

Table 2.3 is a comparison of the near-room temperature rf sputtering parameters employed by Fortunato et al. 2004a,b & 2005 and Carcia 2003. It is interesting to note that these process recipes are distinctly different, even though both groups are pursuing the same objective, namely, to obtain high resistivity, transparent ZnO layers. Carcia et al.'s approach involves the use of low power & high pressure (diffusive transport plasma regime (Smith 1995)), whereas Fortunato et al. choose a relatively high power and low pressure (ballistic transport plasma regime (Smith 1995)). A some-

what puzzling aspect of Fortunato et al.'s recipe is that no oxygen is intentionally introduced into the sputter gas flow. It is likely that the lack of a load-lock on their sputtering system or perhaps a small vacuum leak is supplying the extra oxygen necessary to obtain a low carrier concentration ZnO film with excellent transparency. Fortunato et al. accomplish process optimization with respect to applied rf power by monitoring the resistivity of ZnO films as a function of rf. They choose an optimal power of 100 W, corresponding to a maximum resistivity of 10^8 Ω-cm.

Table 2.3. A comparison of near-room temperature rf magnetron sputtering processes reported by Carcia et al. 2003 and Fortunato et al. 2004a,b, & 2005.

Process parameter	Carcia et al.	Fortunato et al.
Power density (W cm^{-2})	0.5	5
Sputtering gas	Ar:O_2	Ar
Total pressure (mTorr)	20	1
O_2 partial pressure (mTorr)	0.02	0
Target-to-substrate distance (cm)	7.6	10

The reported performance of Fortunato et al.'s ZnO TTFTs is excellent: average optical transmission (including the glass substrate) of 84%, enhancement-mode behavior with a threshold voltage (actually this is the turn-on voltage) of 1.8 V, a field-effect mobility of 70 $cm^2\ V^{-1}s^{-1}$, a gate voltage swing of 0.68 V/decade, and a drain current on-to-off ratio of 5 X 10^5 (Fortunato et al. 2004a).

However, their reported mobility value appears suspect, for several reasons. First, they identify their mobility as a 'field-effect' mobility, and yet indicate that their extraction procedure actually corresponds to that used for saturation mobility assessment. Second, their actual mobility cannot be confirmed directly from their paper since they do not include a drain current-drain voltage plot. Third, their subsequent ZnO TTFT papers (Fortunato et al. 2004b & 2005) do indeed report their estimated mobilities as 'saturation' mobilities, but of smaller magnitudes, i.e., 20 $cm^2\ V^{-1}s^{-1}$ and 27 $cm^2\ V^{-1}s^{-1}$. Fourth, their TTFTs are fabricated in such a manner that the channel is unpatterned, which means that peripheral current will flow outside of the drawn channel defined by the channel width, W, and length, L, due to fringing electric fields (Hong et al. 2007). Evidence for peripheral currents is present in two of their subsequent papers (Fortunato et al. 2004b & 2005), in which they demonstrate a strong increase in μ_{SAT} with decreasing width-to-length ratio, W/L. Although they interpret this μ_{SAT}-W/L trend as due series resistance, it is more likely that it is actually a

fringing current artifact. This unpatterned channel, fringing current artifact non-ideality is discussed in more detail in Section 5.3.2.

A modeling assessment of fringing current artifacts suggests that channel mobilities may be overestimated by as much as an order of magnitude when the channel is unpatterned (Hong et al. 2007). Fringing current artifacts are particularly pronounced for W/L's less than 10. Note that many researchers appear to have reported high values of mobility using TFTs or TTFTs which have unpatterned channels with small W/L ratios, e.g., $\mu_{FE} \approx$ 80 cm^2 $V^{-1}s^{-1}$when W/L = 4 for a $InGaO_3(ZnO)_5$ TTFT (Nomura et al. 2003). The important message here is that unambiguous assessment of channel mobility requires that the channel layer be patterned in order to eliminate the possibility of fringing current artifacts.

Presley et al. demonstrated a staggered, bottom-gate SnO_2 TTFT using ATO as the gate insulator and ITO as the gate, source, & drain contact (Presley et al. 2004). The SnO_2 channel layer is deposited by rf magnetron sputtering and then rapid thermal annealed in oxygen at 600 ºC. The device is described as operating in enhancement-mode since $V_T \approx +10$ V, but this designation is misleading since $V_{ON} \approx -20$ V. Obtaining a positive threshold voltage is asserted to be quite challenging because of the invariably high electron concentration in the SnO_2 channel layer, independent of how the SnO_2 thin film is prepared. Therefore, the channel resistance is decreased by decreasing the channel thickness to 10-20 nm, thereby increasing the shunt resistance of the channel and facilitating transistor action. Device performance is highlighted by an average visible transmittance corrected for reflectance of ~90% (see Fig. 2.2), a maximum field-effect mobility of 2.0 cm^2 $V^{-1}s^{-1}$, and a drain current on-to-off ratio of 10^5.

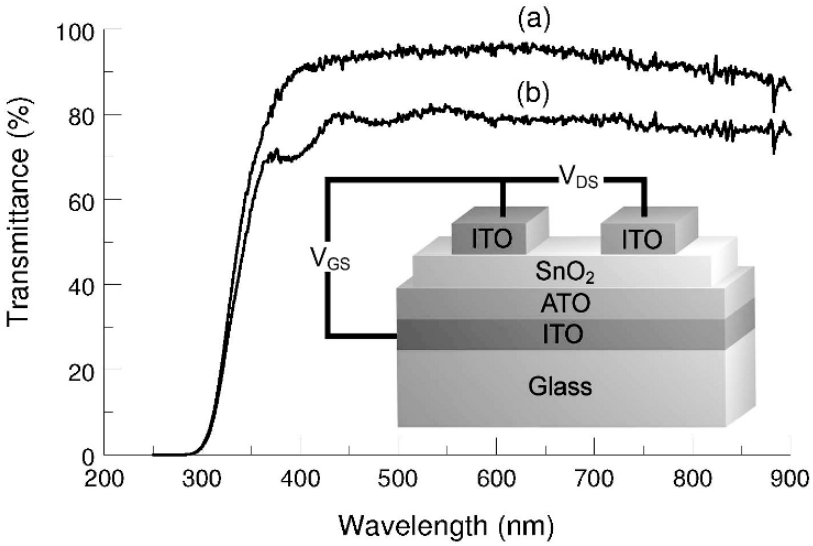

Fig. 2.2. Optical transmittance as viewed through the ITO source/drain and the channel of a SnO_2 TTFT. Curve (a) is corrected for reflectance, i.e. T/(1-R), whereas curve (b) is the raw transmission through the entire stack, including the substrate. Inset illustrates the bottom-gate TTFT and biasing scheme employed. Reused with permission from R E Presley, Journal of Physics D, 37:2810-2813 (2004). Copyright 2004, IOP Publishing Limited.

A significant milestone in the early development of transparent electronics was the demonstration by Nomura et al. of a TTFT on a flexible substrate using near-room temperature processing (Nomura et al. 2004b). This was also the first example of the use of an amorphous multicomponent heavy metal cation oxide (a-MHMC) as a TTFT channel layer. [Note: Instead of using a-MHMC as an abbreviation for these types of oxides, as originally proposed by Hosono et al., we will employ the designation amorphous oxide semiconductor (AOS), since in conventional English parlance the terms 'heavy metal' connote toxicity, which is not the case for all of the materials in this class.] The channel layer, a 30 nm thick amorphous indium gallium zinc oxide (a-IGZO), is deposited by PLD at room temperature onto a 200 μm thick polyethylene terephthalate substrate. Next, a ~140 nm thick Y_2O_3 gate dielectric is deposited and patterned, after which ITO gate, source, and drain electrodes are formed in a coplanar, top-gate device structure. These TTFTs exhibit a saturation mobility of 6-9 $cm^2\ V^{-1}s^{-1}$, a positive threshold voltage of ~1-2 V, a drain current on-to-off ratio of $\sim 10^3$, and are stable during repetitive bending of the TTFT

sheet. Although the drain current-drain voltage curves are not quite ideal, since they do not completely saturate, their electrical characteristics appear to be completely adequate for most TTFT applications, both before and after the application of a bending stress.

Almost a decade before employing a-IGZO as a TTFT channel layer, Hosono et al. pointed out advantages of AOSs for TCO applications (Hosono et al. 1996a,b). Amorphous materials are very attractive from a manufacturing point-of-view because their preparation can typically be accomplished at relatively low temperatures, they tend to have very smooth surfaces, which is advantageous for process integration, and they possess no grain boundaries and the associated pitfalls thereof. However, in 1996 when these papers were published, the electrical performance of amorphous materials was thought to be inherently poor, at least if silicon is considered to be a reliable guide. Hosono et al. contend that electronic transport in an AOS is distinctly different from that of silicon or of a similar covalent semiconductor because a covalent material has strongly-directed sp^3 bonds, in contrast to an AOS with post-transition metal cations whose conduction band minima are derived from isotropic and spatially expanded 4s, 5s, or 6s atomic states. Thus, this difference in bonding leads to better electronic transport, with AOSs possessing mobilities in excess of 10 $cm^2 V^{-1}s^{-1}$ compared to ~1 $cm^2 V^{-1}s^{-1}$ for a-Si. An additional advantage of AOSs is their oxide nature, leading to air processability and thermodynamic stability.

Several aspects of a-IGZO are of general interest in the context of AOSs, as well of a specific interest to this material system as a high-performance TTFT channel material.

First, the Hall mobility of a-IGZO increases with increasing carrier concentration. This trend is at first puzzling, since a higher doping concentration implies increased ionized impurity scattering which would lead to decrease in the mobility. However, this increasing mobility at higher doping concentration trend which is observed for a-IGZO is well known for polycrystalline semiconductors. It is ascribed to a rise in the Fermi level position with increasing doping concentration, resulting in a reduction in the potential barrier seen by conduction band electrons due to grain boundaries, which are modeled as back-to-back Schottky barriers (Hartnagel et al. 1995; Kuo 2004b; Hossain et al. 2003). Remarkably, single crystal IGZO also exhibits this same tendency in which the mobility increases with increasing doping concentration. Nomura et al. explain this *single crystal* trend using a percolation conduction model in which the potential barriers

impeding electron transport are not attributed to grain boundaries but, rather, are ascribed to conduction band edge barriers associated with the random distribution of Ga^{+3} and Zn^{+2} ions in the crystal (recall that a single crystal $InGaO_3(ZnO)_5$ lattice is envisaged as consisting of alternating stacked layers of InO_2^- and $GaO(ZnO)_5^+$ blocks) (Nomura et al. 2004a). In an analogous fashion, the observed a-IGZO trend in which the mobility increases with increasing doping concentration in an *amorphous* material is accredited to a percolation conduction model in which tail state potential barriers arise from the random amorphous bonding structure (Nomura et al. 2004b). It is likely that this mobility versus carrier concentration trend has TTFT device consequences which have not yet been fully appreciated.

Two other a-IGZO properties merit brief mention. First, it is reported that the amorphous phase of IGZO is thermally stable in air up to ~ 500 ºC (Nomura et al. 2004b). This is important from a material/device stability point-of-view and also from the perspective of appreciating the value of an amorphous material and recognizing that many materials, e.g. ZnO, cannot be prepared as an amorphous phase. Second, Nomura et al. 2004b underscore the importance of choosing a TTFT channel material in which the carrier concentration can be reduced to a very low level, ideally $< \sim 10^{14}$ cm^{-3}, in order to achieve a low off current and a large drain current on-to-off ratio. With this objective in mind, they note that the incorporation of Ga ions into a-IGZO is crucially important since this leads to a suppression of oxygen vacancies due to the formation of stronger Ga-O bonds than In-O and Zn-O bonds.

2.1.3 Transparent electronics - 2005

Ten transparent electronics related publications appeared in 2005, involving ZnO TFTs & TTFTs (Carcia et al. 2005; Fortunato et al. 2005; Kim et al. 2005; Yao and Li 2005), AOS TTFTs (Chiang et al. 2005; Dehuff et al. 2005; Jackson et al. 2005; Hong and Wager 2005), electrical device modeling (Hoffman 2005), and the realization of a p-LaCuOSe/n-$InGaZn_5O_8$ blue light-emitting diode (Hiramatsu et al. 2005). Seven of these papers are overviewed in this subsection.

Approximately one month after Nomura et al.'s report of an a-IGZO TTFT on a flexible substrate (Nomura et al. 2005), Chiang et al. demonstrated another AOS TTFT channel layer, zinc tin oxide (ZTO) (Chiang et al. 2005). Two types of bottom-gate, staggered test structures are employed, using a glass substrate with an ATO insulator for the construction

of TTFTs or, alternatively, using a heavily doped silicon wafer substrate with a thermal SiO_2 gate dielectric to fabricate developmental TFTs. The ZTO channel layer is formed using rf magnetron sputtering and post-deposition furnace annealing. Highlights of this work include field-effect mobilities of 5-15 $cm^2\ V^{-1}s^{-1}$ and 20-50 $cm^2\ V^{-1}s^{-1}$ for post-deposition anneals of 300 ºC and 600 ºC, respectively, and corresponding turn-on voltages of 0-15 V and -5-5 V. The drain current on-to-off ratio is typically greater than 10^7. A surprising aspect of this work is that although two different ceramic sputtering targets are used, which are prepared by different suppliers (Oregon State University and a commercial supplier) using different $ZnO:SnO_2$ molar ratios (2:1 and 1:1), the TTFT characteristics are quite similar. This target compositional insensitivity would appear to bode well for manufacturability. ZTO layers are observed to have very smooth surfaces, and to be amorphous, or perhaps nanocrystalline with a maximum crystal size of ~5 nm as estimated from a Scherrer analysis of x-ray diffraction (XRD) peak widths.

Three months later, Dehuff et al. described yet another AOS TTFT channel layer, zinc indium oxide (ZIO) (Dehuff et al. 2005). Using a similar development strategy as reported by Chiang et al. 2005, these ZIO TTFTs are reported to be highly transparent with ~85% optical transmission in the visible portion of the electromagnetic spectrum. When annealed at 600 ºC, ZIO TTFTs are found to operate in depletion-mode with threshold voltages -20 to -10 V and turn-on voltages ~3 V less than the threshold voltage. These devices exhibit excellent drain current saturation, peak incremental mobilities of 45-55 $cm^2\ V^{-1}s^{-1}$, drain current on-to-off ratios of $\sim 10^6$, and subthreshold swings of ~0.8 V/decade. Alternatively, when annealed at 300 ºC, ZIO TTFTs are typically found to operate in enhancement-mode with threshold voltages 0 to 10 V and turn-on voltages ~1-2 V less than the threshold voltage, to also exhibit excellent drain current saturation, peak incremental mobilities of 10-30 $cm^2\ V^{-1}s^{-1}$, drain current on-to-off ratios of $\sim 10^6$, and subthreshold swings of ~0.3 V/decade. XRD analysis indicates that ZIO films are amorphous (or nanocrystalline) for annealing temperatures up to at least 500 ºC. XRD patterns for ZIO thin films display two broad peaks occurring at $2\theta \approx 32^\circ$ and $2\theta \approx 58^\circ$ corresponding to scattering at metal-metal and metal-oxygen interatomic distances, respectively. [Corresponding ZTO broad XRD peaks occur at $2\theta \approx 34^\circ$ and $2\theta \approx 59^\circ$ (Chiang et al. 2005).] Mobility versus gate voltage trends are reported for TTFTs annealed at both 300 ºC and 600 ºC. Both types of devices exhibit a decrease in mobility at large V_{GS}, which is attributed to either an electron injection barrier or interface roughness scattering. Non-optimized ZIO TTFTs fabricated at near room temperature, i.e., with no in-

tentional substrate heating, are found to have a best-case peak incremental mobility of 8 $cm^2\ V^{-1}s^{-1}$ (17 $cm^2\ V^{-1}s^{-1}$) and a drain current on-to-off ratio of 10^4 (3 X 10^3) for enhancement-mode (depletion-mode) operation.

Jackson et al. fabricated ZTO TFTs onto flexible substrates (Jackson et al. 2005). These devices are bottom-gate, staggered TFTs which are constructed onto stainless-steel backed 50 μm thick polyimide sheets. Sputtered Al is employed as a bottom-gate metal and plasma-enhanced chemical vapor deposited silicon oxynitride at a substrate temperature of 300 ºC is used as the gate dielectric. The ZTO channel layer with a 1:1 molar ratio of ZnO to SnO_2 is sputter deposited at near-room temperature and then subjected to a post-deposition anneal at 250 ºC in air. Finally, either Al or ITO is used as the source and drain electrode material. The Al source/drain electrodes are found to be unsuitable, leading to an unacceptably large contact resistance of ~30 kΩ. ZTO TFTs with ITO electrodes are found to yield much better performance: V_T ~ -8.8 V, V_{ON} ~ -17 V, subthreshold swing ~ 1.65 V/decade, drain current on-to-off ratio ~10^6, and μ_{INC} ~14 $cm^2\ V^{-1}s^{-1}$. Although the threshold voltage and subthreshold characteristics of these TFTs are identified as requiring further improvement, this accomplishment demonstrates the potential of ZTO TFTs for flexible electronics applications.

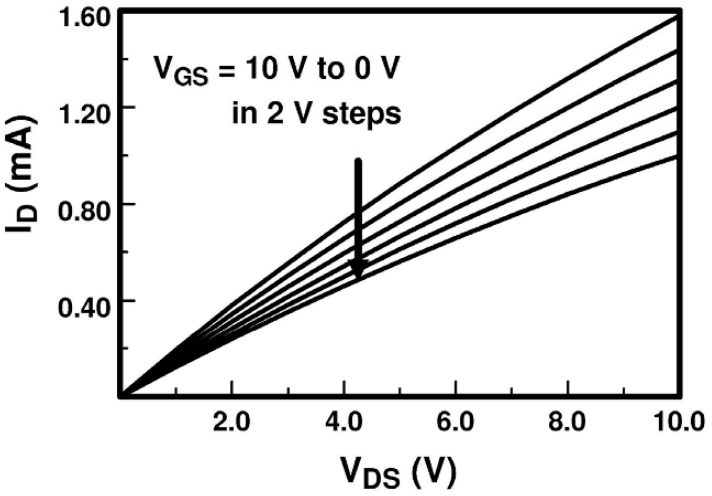

Fig. 2.3. Drain current-drain voltage characteristics of a ZTO TFT which is capped with an ~100 nm thick, thermally evaporated SiO_2 layer. Reprinted with permission from Hong D, Wager JF (2005) Passivation of zinc tin oxide thin-film transistors. J Vac Sci Technol B 23:L25-L27. Copyright 2005, American Institute of Physics.

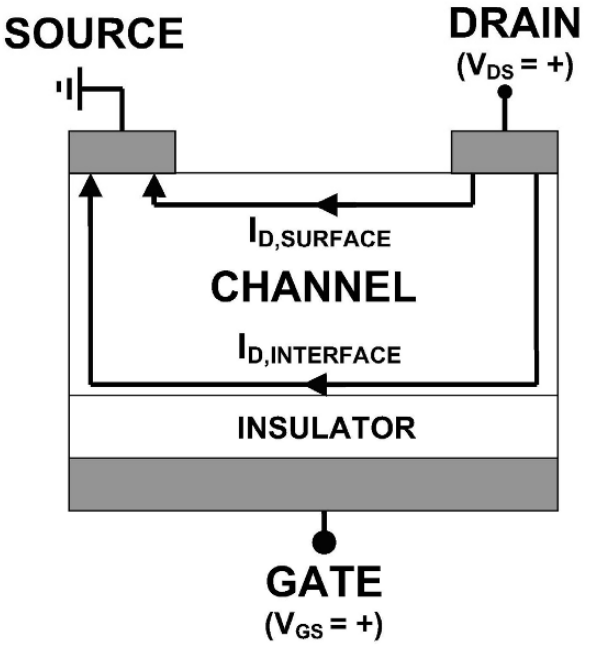

Fig. 2.4. Schematic of a bottom-gate TFT, illustrating current paths that contribute to the overall current in a TFT. $I_{D,INTERFACE}$ is the drain current due to induced carriers from an applied gate bias at the channel layer-gate insulator interface. $I_{D,SURFACE}$ is the drain current due to an electron accumulation layer at the channel layer-passivation layer interface; this contribution degrades the performance of a TFT. Reprinted with permission from Hong D, Wager JF (2005) Passivation of zinc tin oxide thin-film transistors. J Vac Sci Technol B 23:L25-L27. Copyright 2005, American Institute of Physics.

Hong and Wager developed a processing methodology leading to effective passivation of a ZTO surface (Hong and Wager 2005). They find that the drain current-drain voltage characteristics of a ZTO bottom-gate TFT are severely degraded, as illustrated in Fig. 2.3, when an overlayer is deposited onto an air-exposed ZTO top surface. The presence of the overlayer leads to the device performing as a nonlinear gate-controlled resistor, rather than a transistor, since it cannot be turned off and the drain current does not saturate, as indicated in Fig. 2.3. In contrast, a ZTO TFT with an air-exposed surface exhibits qualitatively ideal drain current-drain voltage curves. This overlayer-induced degradation is ascribed to the formation of a surface electron accumulation layer and concomitant shunting of the gate-voltage induced interface conduction current by the surface accumu-

lation layer, as illustrated in Fig. 2.4. Successful passivation of the ZTO surface is accomplished by annealing the TFT after channel layer deposition and an additional anneal after thermal evaporation of a silicon dioxide, calcium fluoride, germanium oxide, strontium fluoride, or antimony oxide passivation layer.

Carcia et al. extended their low-temperature ZnO thin-film synthesis work (Carcia et al. 2003), and demonstrated ZnO TFTs on flexible substrates (Carcia et al. 2005). A highlight of this work is the fabrication of a bottom-gate, coplanar ZnO TFT on a flexible Kapton substrate using Al as the gate, source, and drain contacts, a 400 nm thick electron beam evaporated Al_2O_3 gate insulator, and a 50 nm thick sputtered ZnO channel layer. All of the layers used are deposited near room temperature. This device is asserted to have a 'field-effect' mobility of ~50 $cm^2\ V^{-1}s^{-1}$, although the mobility extraction method mentioned in this paper indicates that it is actually a 'saturation mobility' that is being reported. In any event, this work is further evidence of the potential of inorganic oxides such as ZnO for flexible electronics applications, which require low-temperature processing.

Hoffman extended his previous TFT modeling work (Hoffman 2004) to the development of a closed-form DC model for long-channel TFTs which explicitly accounts for the gate voltage-dependent mobility typically observed in TFTs & TTFTs (Hoffman 2005). An intermediate quantitative result from this modeling effort casts the drain current, I_D, as

$$I_D = C_G \frac{W}{L} \int_{V_{GS}-V_{ON}-V_{DS}}^{V_{GS}-V_{ON}} \mu_{AVG}(V_{eff}) V_{eff}\, dV_{eff}\,, \tag{2.1}$$

where C_G is the gate capacitance density, W is the gate width, L is the gate length, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, V_{ON} is the turn-on voltage, and V_{eff} is the portion of the applied gate voltage that induces mobile channel charge and is given by,

$$V_{eff}(y) = V_{GS} - V_{ON} - V(y)\,, \tag{2.2}$$

where y refers to the distance along the channel with respect to the edge of the source electrode. The important point to note with regard to Eqs. 2.1 and 2.2 is that this model depends critically upon the use of V_{ON} and μ_{AVG}, as defined previously (Hoffman 2004), and could have not been formulated without these quantities. To assess I_D quantitatively, μ_{AVG} (V_{GS}) is extracted from a measurement of the channel conductance in the linear re-

gime of device operation and is expressed as an n^{th} order polynomial curve fit. As examples of model validation, several sets of ZnO and ZTO TFT curves are analyzed and a strong case is presented that the observed reduction in μ_{AVG} at high V_{GS}'s for a ZTO TFT is due to a mobility degradation rather than contact resistance.

Hiramatsu et al. fabricated a pn heterojunction light-emitting diode consisting of an epitaxial p-LaCuOSe layer and an amorphous n-$InGaZn_5O_8$ layer (Hiramatsu et al. 2005, Hiramatsu et al. 2006). Oxychalcogenides such as LaCuOSe are very interesting p-type materials with a structure consisting of alternating stacks of $(Ln_2O_2)^{2+}$ and $(Cu_2Ch_2)^{2-}$ layers, where Ln = lanthanide and Ch = chalcogen, which possess two-dimensional electronic properties similar to those of a modulation-doped superlattice. An undoped LaCuOSe film has a very large hole mobility of 8 $cm^2\ V^{-1}s^{-1}$, similar to that of p-GaN:Mg, while Mg-doping of LaCuOSe can render this material strongly degenerate, with a hole concentration $>10^{20}$ cm^{-3}, and yet it still retains a respectable mobility of ~4 $cm^2\ V^{-1}s^{-1}$. Blue electroluminescence peaking at ~430 nm is observed from this inorganic light-emitting diode at a forward voltage of ~ 8 V, corresponding to a current density of ~1.4 A cm^{-2}. Electroluminescence is attributed to radiative decay of excitons formed in the p-LaCuOSe layer due to electron injection from the n-$InGaZn_5O_8$ layer. Although there are many materials, device, and manufacturing challenges remaining to be overcome before inorganic light-emitting diodes such as these are ready for 'prime time' applications, we believe that this light-emitting diode demonstration is a tremendously important proof-of-concept in the quest for a transparent inorganic display.

2.1.4 Transparent electronics - 2006

Of the twenty-three transparent electronics-related papers appearing in 2006 up to when this review of prior work was completed, i.e., early December 2006 (Barquinha et al. 2006a,b; Görrn et al. 2006; Hiramatsu et al. 2006; Hirao et al. 2006; Hoffman 2006; Hong et al. 2006a,b; Hosono et al. 2006; Hsieh and Wu 2006a,b; Jackson et al. 2006; Lee et al. 2006a,b,c; Matsuzaki et al. 2006; Navamathavan et al. 2006; Ohtomo et al. 2006; Park et al. 2006; Presley et al. 2006; Wang et al. 2006; Yabuta et al. 2006; Yaglioglu et al. 2006), eighteen are briefly reviewed in this subsection.

Matsuzaki et al. fabricated a top-gate TTFT appropriate for applications in the deep ultraviolet portion of the electromagnetic spectrum using Ga_2O_3 as the channel material (Matsuzaki et al. 2006). Ga_2O_3 is appropri-

ate for deep ultraviolet applications since its optical bandgap for direct allowed transitions is very large, i.e., it is estimated to be ~4.9 eV. The Ga_2O_3 channel layer is grown epitaxially by PLD on an α-Al_2O_3 substrate using optimized processing parameters, i.e., 500 ºC $\leq T_{substrate} \leq$ 550 ºC and 5 X $10^{-4} \leq P_{oxygen} \leq 1$ X 10^{-3} Pa. The TTFT operates in depletion-mode with V_T = -6.7 V and a 'saturation field-effect mobility' = 5 X 10^{-2} cm^2 $V^{-1}s^{-1}$, a mobility which is approximately one order of magnitude less than the bulk Hall mobility reported for β- Ga_2O_3.

Lee et al. employed spin-coating synthesis to realize $Zn_{1-x}Zr_xO$ ($0 \leq x \leq 0.10$) bottom-gate TFTs at an annealing temperature of 500 ºC (Lee et al. 2006a). $Zn_{1-x}Zr_xO$ channel layers are synthesized using zinc acetate and zirconium isopropoxide precursors, a bake at 400 ºC immediately after spin-coating, and a final 500 ºC furnace anneal in oxygen. Zr doping of ZnO is used to decrease the channel layer carrier concentration. XRD analysis of Zr-doped channel layers indicates them to have the hexagonal wurtzite structure, with no evidence of ZrO_2. The addition of Zr is found to reduce the grain size (from 50 to 10 nm), the film rms surface roughness (from 44 to 6 nm), the saturation mobility (from 0.4 to 0.03 cm^2 $V^{-1}s^{-1}$), and the carrier concentration (from 5 X 10^{17} to 2 X 10^{16} cm^{-3}); to increase the drain current on-to-off ratio (from less than 10 to greater than 10^6); and to make the turn-on voltage less negative (from immeasurably large and negative to -50 V).

Navamathavan et al. have examined the stability of ZnO TFTs via electrical bias stress testing (Navamathavan et al. 2006). Bottom-gate ZnO TFTs in which the ZnO layer is deposited by rf magnetron sputtering at 350 ºC with a silicon nitride gate dielectric that is deposited by PECVD at 300 ºC are subjected to moderate constant voltages at both gate voltage polarities for a stress duration of 200 s. Significant degradation of the electrical performance is noted even under moderate stressing conditions. Most notably, the drain current on-to-off ratio decreases from 10^5 to 10^2. Additionally, the subthreshold swing increases after stressing. These results suggest that silicon nitride is not an appropriate insulator for oxide-based electronics, even though it is the dielectric-of-choice for a-Si TFTs (silicon nitride and other gate dielectric choices are discussed in Chapter 6).

Hoffman explored stoichiometry and processing temperature effects related to the performance of ZTO TFTs (Hoffman 2006). Using turn-on voltage, V_{TO}, and peak incremental mobility, $\mu_{INC,PEAK}$, as electrical performance figures-of-merit, he concludes that ZTO layers with intermediate

cation concentrations, i.e., Zn/(Zn+Sn) ≈ 0.3-0.7, subjected to post-deposition annealing at ~400-600 ºC are promising for TFT & TTFT applications since such processing results in a relatively high mobility $\mu_{INC,PEAK}$ ~ 25-30 $cm^2V^{-1}s^{-1}$ and near-ideal turn-on characteristics V_{TO} ~ 0 V.

Barquinha et al. investigated the effects of ultraviolet and visible light irradiation on the performance of bottom-gate amorphous zinc indium oxide (a-ZIO) TTFTs in which the channel layer is prepared at near-room temperature by RF magnetron sputtering. (Barquinha et al. 2006a). In the dark, these TTFTs exhibit clockwise hysteresis in log (I_{DS})-V_{GS} transfer curves, consistent with electron trapping in the channel or channel/insulator interface (see Chapter 5 for a discussion of hysteresis). The log (I_{DS})-V_{GS} characteristics are affected by visible and ultraviolet light, with the effect being more pronounced at shorter wavelength, i.e., especially at green and shorter wavelengths. Notably, the amount of hysteresis increases with shorter wavelength and also with increasing irradiation intensity. This work suggests that the properties of low-temperature a-ZIO need to be improved in order for this material to be a suitable choice for transparent electronics applications.

Barquinha et al. studied the effect of channel thickness on the performance of bottom-gate amorphous zinc indium oxide (a-ZIO) TTFTs in which the channel layer is prepared at near-room temperature by RF magnetron sputtering. (Barquinha et al. 2006b). They find for channel thicknesses between 15-60 nm that the threshold voltage decreases, the drain current on-to-off ration decreases, the channel mobility decreases, and the subthreshold swing increases with increasing channel thickness. These channel thickness trends are ascribed to having fewer free electrons in the channel layer and a closer physical proximity of the ungated surface to the accumulation channel with decreasing channel thickness. It does not appear that the channel layers are patterned for the devices employed in this study; it is not clear whether this consideration is pertinent in establishing the channel layer thickness trends observed, but this does not appear likely since the TFT width-to-length ratio is 15 for the devices studied (see Chapter 5 for a discussion of non-patterned channel layer artifacts).

Hirao et al. demonstrated a 1.46” diameter active-matrix liquid-crystal (AMLCD) display in which top-gate ZnO TFTs are used as the pixel switching elements (Hirao et al. 2006). Polycrystalline ZnO is prepared using RF magnetron sputtering from a ceramic target at a substrate temperature of 150 ºC. PECVD SiN_x deposited at a substrate temperature of

250 ºC serves as the gate dielectric and Cr is used as the source, drain, and gate electrode in a coplanar structure. The maximum substrate temperature used to fabricate these ZnO TFTs is 250 ºC. The ZnO TFTs are reported to have a field-effect mobility of 50.3 $cm^2 V^{-1}s^{-1}$, a threshold voltage of 1.1 V, a drain current on-to-off ratio of 4.6 X 10^6, and a subthreshold swing of 210 mV/decade. The AMLCD display fabricated has 61,600 pixels (220 vertical X 280 horizontal).

Hsieh and Wu studied the effect of gate length (2-50 μm) and width (20-200 μm) scaling for ZnO TTFTs (Hsieh and Wu 2006a,b). Their ZnO TTFTs are bottom-gate devices with a staggered structure in which ITO is used for the source, drain, and gate electrode. Either RF sputtered Al_2O_3 or HfO_2 is used as the gate insulator. Al_2O_3 is found to yield reduced gate leakage current because of its wide band gap while HfO_2 gives better device performance due to its superior interface properties. The channel layer is 180 nm thick ZnO deposited by RF sputtering and subjected to a 265 ºC post-deposition anneal in nitrogen. ZnO TTFT performance is highlighted by a saturation mobility of 8.4 $cm^2 V^{-1}s^{-1}$, a threshold voltage of 4.3 V, a drain current on-to-off ratio of ~10^7, and a subthreshold swing of 950 mV/decade. Device performance is found to be well-behaved down to a channel length of ~ 5 μm. However, short-channel effects (a decrease in threshold voltage, an increase in subthreshold swing, and loss of hard saturation) are observed for a channel length less than ~ 5 μm. One questionable aspect of this study, however, is that an anomalously large channel thickness of 180 nm is employed; it is likely that short-channel effects will be less pronounced if the channel layer thickness is reduced to a more typical value of ~30-60 nm.

Park et al. used ZnO TTFTs to fabricate a 2.15" 176 X 144 [106 dots per inch (dpi)] active-matrix organic light-emitting device (AMOLED) display demonstration (Park et al. 2006). Their ZnO TTFTs are bottom-gate, staggered devices in which the Al_2O_3 gate, the ZnO channel, and the ZnO:Al layers are all deposited via atomic layer deposition (ALD) at a maximum substrate temperature of 250 ºC. ALD ZnO layers deposited below 300 ºC are found to have a (100) crystalline orientation, rather than the more conventional (002) orientation, and are reported to be nanocrystalline without a dead layer. ZnO TTFT performance is summarized as having a field-effect mobility of 1.13 $cm^2 V^{-1}s^{-1}$, a threshold voltage of 0.8 V, a drain current on-to-off ratio of ~10^6, and a subthreshold swing of 1.65 V/decade. An AMOLED display is constructed using two ZnO TTFTs and a capacitor to drive each OLED pixel. OLEDs are fabricated via vacuum evaporation using a NPD/Alq/LiF/Al/Ag stack. The relatively large

resistance of the ITO, compared that of a metal interconnect, led to a gradient in the luminance of the AMOLED. Another transparent backplane problem noted is the high sheet resistance of the ZnO:Al source/drain electrode (90 Ω/square).

Görrn et al. realized a fully transparent smart pixel by stacking an OLED onto an a-ZTO TTFT (Görrn et al. 2006). The a-ZTO TTFT has a bottom-gate, staggered device structure using ITO as the gate electrode, ATO as the gate dielectric, PLD-deposited ($T_{substrate}$ = 350 ºC) a-ZTO as the channel layer, and ZnO:Al source/drain contacts. The a-ZTO TTFT has a field-effect mobility of 11 $cm^2 V^{-1}s^{-1}$, a threshold voltage of -1 to +1 V, a drain current on-to-off ratio of ~10^5, and no hysteresis in the transfer curves. The OLED is a complicated 9-layer stack deposited by organic molecular beam epitaxy which is stacked directly on top of the drain electrode. ITO is used as the OLED top contact. Sputter damage during deposition of the top contact is noted as leading to a decrease in OLED efficiency. The smart pixels are highly transparent, more than 70% in the visible portion of the electromagnetic spectrum.

Presley et al. fabricated transparent integrated circuits - inverters and ring oscillators - using amorphous indium gallium oxide (a-IGO) as a channel material (Presley et al. 2006). A staggered, bottom-gate configuration is employed, using ITO as the gate, source, and drain contact and the interconnect, PECVD SiO_2 as the gate dielectric, and RF magnetron sputtered a-IGO post-deposition annealed at 500 ºC as the channel layer. The a-IGO TTFT has a peak incremental mobility of ~7 $cm^2 V^{-1}s^{-1}$, a turn-on voltage of ~2 V, a drain current on-to-off ratio of ~10^4, and a small amount of hysteresis in the transfer curves (V_{ON} between forward and reverse sweeps varies less than 1 V). Inverters are constructed by connecting a control TTFT (W/L = 40) in series with a load TTFT (W/L = 10). Inverter transfer curves yield a maximum gain of 1.5. A ring oscillator is an odd combination of inverters connected in series, whose realization constitutes a simple integrated circuit (IC) validation and whose performance is indicative of the expected frequency performance of an IC technology. Presley et al. demonstrate a five-stage ring oscillator exhibiting a maximum oscillation frequency of ~9.5 kHz (~2.2 kHz) with the gate and drain biased at 80 V (30 V). Since the ring oscillator circuit employed is designed using very large device dimensions and gate overlap, leading to large transit times and excessive parasitic capacitance, this report should be construed as a materials proof-of-concept demonstration, rather than a reflection of the ultimate frequency performance of this technology.

Ohtomo et al. compared the performance of ZnO and $Mg_xZn_{1-x}O$ TFTs in terms of their photoresponse characteristics (Ohtomo et al. 2006). They observe a deleterious change in the drain current-gate voltage transfer characteristics of a ZnO (bandgap = 3.27 eV) TFT when it is exposed to 400 nm light, which they attribute to photoexcitation involving band tail states. In contrast, TFTs with $Mg_{0.1}Zn_{0.9}O$ (bandgap = 3.47 eV) or $Mg_{0.3}Zn_{0.7}O$ (bandgap = 3.8 eV) channel layers exhibit a negligible photoresponse. $Mg_{0.1}Zn_{0.9}O$ is preferred to $Mg_{0.3}Zn_{0.7}O$ as a channel layer since it has negligible photoresponse and superior TFT electrical performance.

Yabuta et al. reported on the fabrication of top-gate a-IGZO TFTs by rf magnetron sputtering at near room temperature (Yabuta et al. 2006). These devices are deposited onto unheated substrates in which the substrate temperature rises during sputtering to 40 ºC and 140 ºC, respectively, after deposition of the a-IGZO channel layer and the Y_2O_3 gate insulator. The performance of these TFTs is excellent, highlighted by a field-effect mobility of 12 $cm^2\ V^{-1}s^{-1}$, a turn-on voltage of $\sim 0^+$ V, a threshold voltage of +1.4 V, a drain current on-to-off ratio of $\sim 10^8$, and a subthreshold swing of 0.2 V/decade. Thus, this result demonstrates the viability of a-IGZO TFTs when fabricated using sputtering, a well-established manufacturing technology.

Kim et al., Lee et al., and Wang et al. explored the use of alternative insulators as a means of improving the performance of TTFTs (Kim et al. 2006; Lee et al. 2006; Wang et al. 2006). Since the drain current is proportional to the gate capacitance, and the turn-on voltage, threshold voltage, and subthreshold swing are inversely proportional to the gate capacitance, increasing the gate capacitance indeed provides a clear path for improving TTFT performance, if an adequately low gate leakage can be maintained. To this end, Kim et al. used $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$, with a relative dielectric constant of 55 at 1 kHz, as a gate insulator in a ZnO TFT. This work demonstrates aspects of device improvement in terms of low voltage operation, a threshold voltage of 2 V, and a relatively low subthreshold swing of 0.25 V/decade. However, the field-effect mobility is quite low, 0.024 $cm^2\ V^{-1}s^{-1}$, and significant gate leakage begins to flow at a relatively small gate voltage of 4 V, indicating that both the channel layer and the insulator require further optimization. Lee et al. investigated the use of a polymer/high-k oxide double layer gate insulator consisting of spin-coated poly-4-vinylphenol and electron beam evaporated 65% SiO_2-35% CeO_2 mixed oxide with an average relative dielectric constant of ~9.8. This hybrid gate dielectric led to improved TFT performance compared to the exclusive use of a polymer dielectric, but their device performance is still

only marginal with a field-effect mobility of ~0.48 $cm^2\ V^{-1}s^{-1}$ and a drain current on-to-off ratio of ~3 X 10^3 when the ZnO is deposited at 100 ºC. Finally, Wang et al. assert that they obtain excellent TFT performance, i.e., field-effect mobilities >120 $cm^2\ V^{-1}s^{-1}$, near-zero threshold voltages, sub-threshold swings of 90 mV/decade, and drain current on-to-off ratios of ~10^5, when using In_2O_3 deposited by ion-assisted deposition as the channel layer and solution-deposited, self-assembled nanoscale organic gate dielectrics. These results are hard to reconcile with the I_D-V_{DS} curves reported therein (Wang et al. 2006) and in their corresponding papers detailing their dielectric optimization procedure and electrical characteristics (Facchetti et al. 2005, Yoon et al. 2005), since their TFTs clearly suffer from a high degree of gate leakage, as evident from the fact that I_D does not go to zero for various V_{GS}'s when V_{DS} is equal to zero. Our work at OSU indicates that when the gate leakage is this pronounced, the channel mobility may be overestimated by an order of magnitude or more. We have found that the channel mobility can only be reliably estimated when the gate-drain leakage is negligible compared to the drain-source current.

Hong et al. compared the performance of ZTO TFTs in which the channel layer is deposited by dc or rf magnetron sputtering using ceramic or metal targets (Hong et al. 2006b). The significant conclusion of this study is that comparable TFT performance is obtained. This bodes well for transparent electronics, since dc magnetron sputtering using metal targets is preferable for manufacturing.

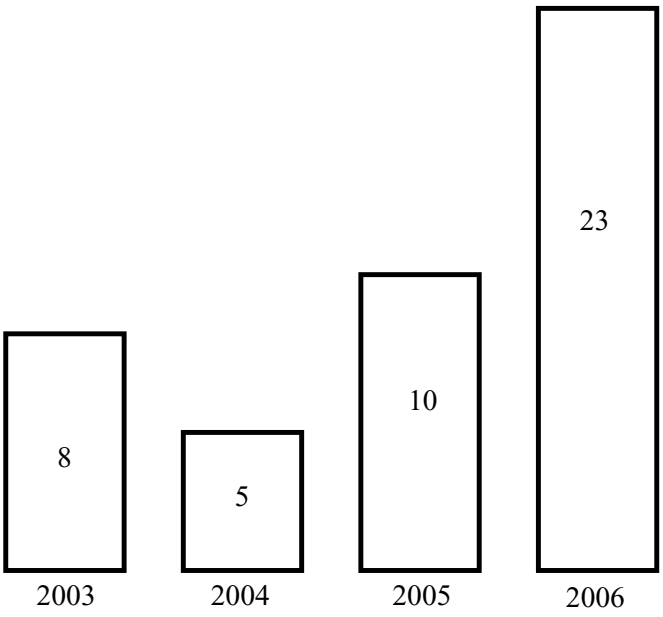

Fig. 2.5 Number of transparent electronics-related papers published per year

2.2 Perspective & Outlook

Figure 2.5 is a bar chart representation of the yearly number of transparent electronics-related papers which have been published since 2003. The time origin is taken as 2003, since this is when the first fully-transparent, electronically functioning transistors were announced publicly. Two aspects of Fig. 2.5 are of interest. First, it is clear that very few papers have been published to date on the topic of transparent electronics. Thus, it appears that a limited amount of research and development effort has been devoted to this topic. Second, if 2006 is any indication, it appears that the amount of interest in transparent electronics is dramatically growing. It is our opinion that this interest is commercially and scientifically warranted, and this book is devoted to fostering and accelerating this interest.

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3 Applications

3.1 Looking into a crystal ball

Writing a chapter on transparent electronics applications is similar to looking into a crystal ball, and trying to decide if you are really seeing something, or if you are just staring at your own reflection. The problem is that transparent electronics applications are not yet defined. In fact, it is unlikely that they are presently even accurately definable due to the current lack of maturity of this technology. Given this excuse, the future reader will please accord the authors of this monograph some slack regarding the probable errant nature of some of the discussion offered in this chapter.

3.2 A technology appraisal

As mentioned in Chapter 1, the availability of transparent conductive oxide (TCO) thin-film coatings has given rise to a mature, and yet still growing multi-billion dollar technology with a very broad and dynamically changing range of applications. Recall that these TCO applications are categorized as *passive* and *electrical*. Conventional wisdom suggests that the market for *active* transparent *electronics* would, at maturity, be significantly larger than that of TCOs, given the inherently much broader range of active electronic compared to passive electrical applications.

Why is this so? To a large extent, the fertility of electronic compared to electrical applications is attributable to the existence of the transistor. The two most important attributes of a transistor are its ability to amplify and to switch. These transistor assets are a consequence of the three-terminal nature of this device; a third terminal offers control which is not possible with a two-terminal device. Transistors are useful in both analog and digital applications. In addition to amplification (e.g., audio, low-noise, differential, operational amplifiers) and switching, transistors are useful for

digital logic (NOT, NAND, NOR gates; programmable logic arrays, decoders, encoders, multiplexers, comparators, arithmetic logic units; latches, flip-flops, shift registers, state machines, read-only and random-access memory), control, oscillator, variable resistor, signal waveshaping, and impedance transformation applications [Ng 2002]. Thus, the existence of a TTFT bodes well for transparent electronics, in terms of leading to a multiplicity of applications.

In addition to TTFT functionality, other properties may play a crucial role in determining future transparent electronics technologies. A specific and likely important example is the ultraviolet (UV) photoconductivity of certain transparent electronics materials, which may facilitate the realization of UV detector arrays and other applications, as discussed in Sections 3.3 and 3.4.

What branch of electronics (e.g., simple switching, digital, analog, power, microwave, etc.) is most suitable for transparent electronics applications? In an attempt to begin to answer this question, it seems appropriate to evaluate perceived strengths and weaknesses of transparent electronics, as summarized in Table 3.1.

Table 3.1. A comparison of perceived transparent electronics strengths and weaknesses.

Strengths	Weaknesses
visible transparency	high resistance of TCOs
large area	low frequency operation
low cost	lack of complementary devices
low temperature processing	technological immaturity
simple device structure	
free real estate	
smooth surfaces	
passive availability (R & C)	
robust, stable inorganic materials	
safe, non-toxic materials	

First, consider the ‘strengths’ listed in Table 3.1.

- Although the inclusion of visible transparency is self-evident, it is explicitly included in this table to underscore the one essential attribute which currently establishes transparent electronics as unique. If visible transparency and electronic functionality are requisite properties, transparent electronics is presently the only possible technological

choice. Transparent electronics appears to be a technology well suited to large-area applications since it involves the use of thin layers onto substrates such as glass and plastic, the manufacturing of which appears readily scalable to extremely large sizes.

- Additionally, transparent electronics offers the possibility of low cost, depending partially on the cost of the substrate, and additionally on whether thin-film deposition and pattern definition is accomplished via physical vapor deposition (PVD) and photolithography (higher cost) or by solution-based deposition and printing (lower cost). The relative cost depends, to a certain extent, on the specific application under consideration and also on the cost structure of all competing technologies. We believe that the performance and reliability of a mature transparent electronics technology offers compelling advantages in the area of low-cost and large-area electronics, even when visible transparency is not a valued attribute.

- Another 'strength' included in Table 3.1 is low temperature processing. 'Low' is a loaded word in the context of processing temperature, and again depends on the specific application and competing activities. We list 'low processing temperature' as an advantage because transparent electronics is assuredly compatible with fabrication on glass substrates and there is compelling early development stage evidence that it is also suitable for use with plastic substrates [Carcia et al. 2003; Nomura et al. 2004b; Carcia et al. 2005; Fortunato 2004a,b].

- 'Simple device structure' refers to the fact that high performance TTFTs can be fabricated with the contact placed directly onto the channel to form the source and drain, without having to intentionally dope these regions in order to make them Ohmic. This is in contrast to MOSFETs, a-Si TFTs, and poly-Si TFTs, but is similar to OFETs.

- 'Free real estate' is an integrated circuit designer's dream, since as much functionality as possible is squeezed out of every silicon IC; i.e., real estate on a silicon wafer is a very valuable commodity. In contrast, we believe that many transparent electronics applications of the future will 'harvest wasted real estate' by the addition of electronic functionality onto surfaces which currently are not used in this manner. For example, an automobile dashboard plastic or glass or a viewing window typically offers physical separation, but no electronic utility.

- ‘Smooth surfaces’ pertains to the use of amorphous channel layers and dielectrics, the approach to transparent electronics that we endorse. A smooth surface is easier to integrate into a device, circuit, or system and also offers the possibility of improved electron transport performance (less interface roughness scattering) and superior reliability (improved electric field uniformity; no grain boundaries, which means less impurity segregation and enhanced diffusion).

- Another potential advantage of transparent electronics is that resistors and capacitors, which are passive components, are easily realizable, thereby increasing the circuit designer’s toolset. It may also be possible to realize inductors in the context of transparent electronics, but inductors are not included in as an explicit strength in Table 3.1 since they will likely be lossy as a consequence of the relatively resistive nature of the TCO used to fabricate the inductor.

- The primary materials employed in transparent electronics are inorganic oxides, which are classified as robust and stable (chemically and physically); this classification is especially relevant when compared to organic or polymer electronic materials.

- The final ‘Strength’ entry included in Table 3.1 is that safe, non-toxic materials will be used. Transparent electronics thin-film materials synthesis will likely be accomplished via physical vapor deposition. Thus, chemical vapor deposition using hazardous gases such as silane, phosphine, arsenine, etc., as are commonly used in silicon-based technologies will not be required. Moreover, the use of heavy metals such as mercury, cadmium, lead, and thallium will be avoided. Our hope, desire, and intent is that transparent electronics will be a relatively `green’ technology.

Perhaps we are biased, but the list of perceived weaknesses included in Table 3.1 is significantly shorter than the list of strengths. However, these transparent electronics liabilities are somewhat debilitating with respect to certain applications. Consider the four weaknesses listed in Table 3.1.

- Perhaps the most important weakness included in Table 3.1 is the high resistance of TCOs. As reported in Chapter 1, TCOs are about 10-60 times more resistive than typical integrate circuit contact metals. This consideration could severely limit many applications. It will be very difficult to run long bus lines across large-area substrates without

suffering significant Joule heating and signal distortion. This consideration is so imposing for many desired transparent electronics applications that we propose to distinguish between two types of transparency; *global* and *local*. Certain applications, e.g., a fully transparent display, require global transparency over the entire area of the system in question. Because of the relatively resistive nature of TCOs, globally transparent applications such as these will be very difficult to realize. They are most readily accomplished when the system area is small, and hence the bus line length may be kept short. Other applications, however, might require visible transparency over a small fraction of the overall system area; such an application is denoted as locally transparent. An example of this type of application is the use of a transparent switch in an AMLCD pixel, as discussed in Section 6.3.4, where the primary purpose of the transparent switch is to improve the pixel fill factor and to simplify the pixel architecture by eliminating the need for light shielding of the switching transistor.

- Operation frequency is another possible 'show stopper' for certain applications. Near-term transparent electronics applications will most likely involve frequencies in the range of kHz to low-MHz. To obtain a perspective on the maximum operation frequency, consider the cut-off frequency, f_T, i.e., the unity-gain frequency under a short-circuit load, for a TTFT in which parasitic gate capacitance is ignored (this is a best-case, but unrealistic situation),

$$f_T = \frac{\mu(V_{GS} - V_T)}{2\pi L^2} \tag{3.1}$$

where μ is the channel mobility, (V_{GS} - V_T) is the gate overvoltage (i.e., the applied gate voltage in excess of the threshold voltage), and L is the gate length. Equation (3.1) shows that, in this approximation, the TTFT operating frequency depends directly on the channel mobility (a material property) and gate overvoltage (determined by the supply voltage and a material property), and inversely on the square of the gate length (determined by the patterning method employed). Assuming an overvoltage of 10 V and a mobility of 10 $cm^2V^{-1}s^{-1}$ yields $f_T \approx 16$ MHz (for L = 10 μm) and $f_T \approx 400$ MHz (for L = 2 μm). For comparison, assuming an overvoltage of 10 V and a mobility of 50 $cm^2V^{-1}s^{-1}$ yields $f_T \approx 80$ MHz (for L = 10 μm) and $f_T \approx 2$ GHz (for L = 2 μm). Although these maximum operating frequency estimates are crude and apply only to idealized discrete devices rather than realistic operating circuits, this comparison does drive home the main point, namely, that certain

applications, e.g., telecommunications, are currently not good candidates transparent electronics realization.

- Current n-channel TTFT (n-TTFT) technology is analogous to classical NMOS silicon technology. The realization of a *p*-channel TTFT is much more difficult than an *n*-channel TTFT. However, the reward, in terms of technological and commercial implications, is *immense* since the availability of *p*- and *n*-channel, enhancement-mode TTFTs makes possible the realization of a transparent CMOS-like technology, which we denote c-TTFT. Such a technology would possess the same advantages as silicon CMOS technology that currently dominates semiconductor electronics, including: (i) low power consumption, (ii) low heat dissipation, (iii) high packing density, (iv) simple circuit architecture, (v) large output voltage swing and hence noise margin, (vi) analog and digital processing on the same substrate with high circuit densities, (vii) simple design(Wolf 1990). The lack of a c-TTFT technology is a severe limitation of current state-of-the-art transparent electronics.

- Lack of technological maturity is a problem faced by all emerging technologies. For a company pondering the commercialization of such a technology, risk is an important downside consideration since hidden material, device, circuit, system, or manufacturing challenges and unexpected 'show-stoppers' are often encountered as a novel product is initially taken to market. The upside is the potential profit associated with being the first to enter the market.

3.3 An application smorgasbord

Prior to discussing specific transparent electronics applications, it is useful to consider the classification scheme shown in Table 3.2. The intent of this table is to provide a bit of organizational structure from which applications may be sorted and assessed. Under each of the four categories included in this table - device functionality, device topology, application type, and application category - is a list of descriptive labels which distinguish a given application from the perspective of the respective category. Note that all of the device functionality labels included in the first column of Table 3.2 refers primarily to TFT functions, except for the last entry, i.e., photoconductor. The remaining categories and category labels which are included in Table 3.2 are relatively self-explanatory, and are clarified by their use in Table 3.3.

Table 3.2. A list of categories corresponding to the classification scheme used in Table 3.3.

Device functionality	Device topology	Application type	Application category
switch	discrete device	display	architectural
amplifier	distributed devices	energy	automotive
control	1D array	hard copy	computer / peripheral
analog	2D array	imaging	industrial / instrumentation
digital	3D array	sensor	consumer
power	integrated circuit	toys, games	communications
photoconductor			medical
			military / aerospace
			security & identification

Next, a list of potential transparent electronics applications is provided in Table 3.3. Each application is described using the classification scheme introduced in Table 3.2. The remainder of this section constitutes a brief discussion of each of the applications included in Table 3.3.

Table 3.3. A list of possible transparent electronics applications and associated classification schemes.

Application	Device functionality	Device topology	Application type	Application category
AMLCD transparent switch	switch	2D array	display	computer / peripheral, consumer
AMOLED backplane	switch, control	2D array	display	computer / peripheral, consumer
transparent CCDs	multiple categories	multiple categories	multiple categories	computer / peripheral, consumer
integrated on-'glass' electronics	multiple categories	multiple categories	multiple categories	computer / peripheral, consumer

Table 3.3 (continued)

Application	Device functionality	Device topology	Application type	Application category
UV detectors & arrays	photoconductor, analog	2D array, distributed devices	sensor, imaging	industrial, instrumentation, medical, military
transparent displays	multiple categories	2D array	display	multiple categories
spatial light modulator	photoconductor	discrete device	display	multiple categories
value-added glass	multiple categories	multiple categories	multiple categories	architectural, automotive
smart windows, smart mirrors	analog	distributed	energy, display	architectural, automotive
transparent solar cells	power	discrete & distributed devices	energy	consumer, architectural
reduced size hard copy unit	photoconductor, analog	2D array, distributed	hard copy	industrial, computer / peripheral
transparent electronics on opaque substrates	multiple categories	multiple categories	multiple categories	architectural, automotive
transparent circuit boards	multiple categories	2D & 3D arrays	multiple categories	computer
optometric applications	multiple categories	multiple categories	multiple categories	medical
x-ray imaging	switch	2D array	sensor, display	medical
security applications	multiple categories	multiple categories	multiple categories	architectural, consumer, military
automotive applications	multiple categories	multiple categories	multiple categories	automotive
military & aerospace applications	multiple categories	multiple categories	multiple categories	military / aerospace
toys, games, art	multiple categories	multiple categories	toys, games, art	consumer

- Active-matrix liquid-crystal display (AMLCD) transparent switch. Most current state-of-the-art LCD displays employ active-matrix addressing in which a transistor is used at each pixel. Today, most AMLCD displays use amorphous silicon (a-Si) TFTs as switching transistors. This proposed transparent electronics application involves the use of a TTFT instead of an a-Si TFT for active-matrix addressing. This application is considered in more detail in Section 6.3.4.

- Active-matrix organic light-emitting device (AMOLED) display backplane. AMOLED displays are beginning to be commercialized. Two main backplane technologies are currently under consideration, a-Si and low-temperature polysilicon TFTs. We contend that transparent electronics is a viable AMOLED backplane option. This application is considered in more detail in Section 6.3.5

- Transparent charge-coupled devices (CCDs). CCDs are used extensively today, primarily in imaging applications, e.g., digital cameras, video cameras, optical scanning, etc., but also as shift registers. A proposed application, not yet reduced to practice, involves the realization of a transparent CCD for imaging and shift registers, and possibly other applications in the areas of digital or analog electronics or signal processing. This application is considered in more detail in Section 6.3.6.

- Integrated on-'glass' electronics. If peripheral electronics for power conditioning, control, addressing, and/or signal transmission could be integrated onto the 'glass' ('glass' since it is recognized that some future applications will employ alternative substrates) substrate of a system, this on-'glass' electronics strategy would offer the possibility of reduced system cost and improved reliability.

  In this context, a primary reason why polycrystalline silicon is currently under intense development for AMLCD and AMOLED applications is that it offers the possibility for integrating more and more peripheral electronics functionality directly onto the glass substrate. This integrated on-'glass' electronics approach has the potential for price reduction due to the cost structure of polysilicon versus single crystal silicon technology, and for improving reliability due to the reduced interconnect, solid-state nature of such a system.

Amorphous silicon (a-Si) technology is also being explored for such applications, but the low channel mobility, NMOS circuit topology, and relatively poor lifetime of a-Si TFTs is not as attractive for on-'glass' electronics as polysilicon technology.

As discussed in more detail in Section 6.3.5, transparent electronics offers an intermediate alternative approach to that of a-Si and polysilicon technology. Several possible on-'glass' electronics application venues exist in the context of AMLCDs: row drivers, column drivers, DC/DC power converters, inverters, timing controllers, data controllers, digital-to-analog converters, etc. (den Boer 2005). Of these, row driver applications appear to be an intriguing possibility since their operating frequency is rather modest, i.e., less than 50 kHz. Integrated on-'glass' electronics for OLED application venues also exist, but at this time appear to be less well defined due to the relative immaturity of this technology.

It is likely that once on-'glass' electronics is a mainstream technology, many new applications will emerge, since this approach offers the attractive possibility of realizing an entire 'system-on-a-substrate'.

- Ultraviolet (UV) detectors and arrays. High quality transparent electronics materials are transparent to visible light, but often strongly absorb in the UV portion of the electromagnetic spectrum. Thus, a transparent electronics platform may be suitable for UV detector applications using either a TTFT or a CCD approach.

  To a certain extent, TTFT and photoconductor applications work in opposition to one another. Ideally, a TTFT absorbs no light at any wavelength, while a photoconductor strongly absorbs light, at least in a certain range of wavelength.

  To get a more quantitative feel for these opposing tendencies, if a 50 nm thick TTFT channel layer has absorption coefficients 10^3 cm^{-1} and 10^5 cm^{-1}, respectively, in the visible and UV portions of the electromagnetic spectrum, the channel layer would absorb 0.5% and 40% of the incident irradiance in these two regions. Thus, a single- or double-gate TTFT with opaque source and drain contacts could potentially function as a UV detector, as long as the channel layer is a poor visible but a good UV photoabsorber.

There are several attractive features of this UV detector realization. First, since the UV detector is a TTFT, electronic sensitivity control and resetting after photoexcitation are feasible. Second, again since the UV detector is a TTFT, active-matrix addressing in conjunction with a storage capacitor is possible, leading to the prospect of a 2D UV detector array. Third, the channel portion of this detector is transparent to visible and infrared light. Therefore, if one or more 2D visible and/or infrared detector arrays are fabricated and aligned below this 2D UV detector array, a tiled spectrally-resolved imaging array could be constructed, which would harvest different portions of the incident electromagnetic spectrum. Fourth, this UV detector & array strategy appears to be inherently low-cost. This cost structure would make them attractive for many industrial UV sensing applications such as position-sensitive detectors, motion detectors, automated inspection, security, etc. (Wilson 2005).

A transparent CCD, as discussed in Section 6.3.6, is an alternative and potentially attractive route to the attainment of UV detector arrays.

- Transparent displays. Hollywood has already clearly revealed the potential utility and appeal of transparent displays.

  In a scene from the 2002 movie, `Minority Report`, Tom Cruise portrays a policeman of the future who frantically manipulates images of `bad guys' on a transparent display while several of his cohorts surrounding him look on from different parts of the room, as do several other collaborators who are teleconferencing from remote locations. [In addition to the very impressive transparent display shown in this scene, someone should also work towards invention of the `magic fingers' which Cruise uses to manipulate these images!]

  Another Hollywood example of a transparent display occurs in a scene from the 2000 movie `Red Planet` in which an astronaut jumps out of a spaceship on Mars and pulls out something that looks like a pen, from which he rolls out a flexible, magnifiable, interactive, transparent imager/map in which the visible Martian terrain is map-highlighted and annotated. It will take several decades of intense R&D before all of the functionality of this transparent display system is fully realized.

  Anyone who does not appreciate the utility of a transparent display is advised to see the relevant scenes in one or both of these movies. We consider a transparent display to be the holy grail of transparent

electronics applications. Note, however, that a transparent display is an extremely challenging application, requiring *global* transparency and robust, full-color, distributed, transparent light sources with long lifetime.

- Spatial light modulator applications. A spatial light modulator (SLM) is an optical device in which an incident beam of light is either electronically or optically addressed so as to produce a spatially varying optical signal output (Efron 1995). SLM applications include optical computing, optical signal processing, and projection displays (Efron 1995; Stupp and Brennesholtz 1999; Robinson et al. 2005). An example of a SLM application involving transparent electronics is indicated in Fig. 3.1, which shows a simplified schematic of a light amplifier that could be used as an optically-addressed SLM light valve in a projection display application (Spiegelberg 2007). A voltage applied across the transparent photoconductor (PC) and the liquid crystal (LC) cell capacitively divides across these layers. Rastered, spatially modulated ultraviolet (UV) light is used to define the spatial transmission of incident visible light through the light valve, since UV is absorbed in the PC layer, shorting out this layer so that the applied voltage drops entirely across the LC cell, thus modulating the transmitted light intensity. In a typical projector display application, three light valves are used, one for each of the primary colors red, green, and blue.

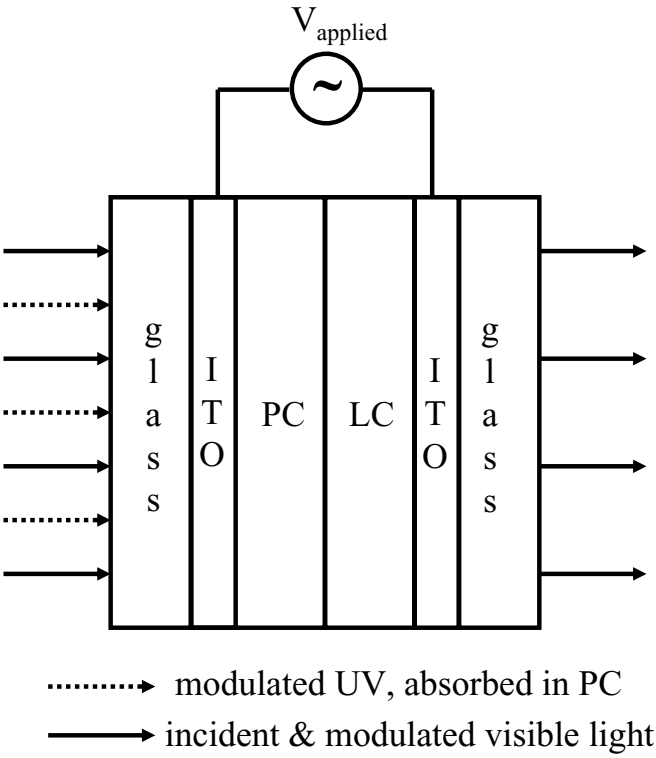

Fig. 3.1. Simplified schematic of a light amplifier employing a transparent photoconductor (PC) in series with a liquid crystal (LC) cell. This light amplifier may serve as an optically-addressed spatial light modulator light valve for projection display applications. Spatial modulation of the incident visible light is accomplished using a rastered beam of ultraviolet (UV) light. Typically, three such light valves would be required for a full-color display, in order to separately modulate the red, green, and blue portions of the visible spectrum. Indium tin oxide (ITO) serves as transparent electrodes for the PC/LC capacitive divider.

- Value-added glass. Glass windows are omnipresent, in homes, buildings, automobilies, trains, planes, etc. From an electronics perspective, glass windows constitute unharvested real estate. In many respects, glass is a very desirable substrate for transparent electronics applications since its processing temperature is comparatively rather high and its surfaces are adequately smooth. However, specific glass substrate-based electronics applications are not yet well defined. Thus, this `value-added glass' category currently serves more as a catch-all, bookmarker reminder of a family of future application opportunites,

rather than as a specific blueprint for immediate product-oriented developmental activity.

Given this caveat, one can envisage forthcoming applications in which touch screen activated maps are available on the passenger viewing window of a train; temperature, humidity, and/or pollution sensors and their corresponding viewable data are incorporated into office windows of a high-rise building; art, advertisement, and/or music is reconfigurably updated in a glass escalator divider in a mall; indicator lights directing airline passenger boarding routes are displayed in various colors indicative of how much time remains before a flight is ready to take off; motion-activated transparent signs displaying reconfigurational information about opening hours are imbedded into glass doors of a museum or other public building; energy is supplied to a building from UV energy harvesting windows, etc. The possiblities appear to be endless, once the transparent electronics paradigm is adopted.

- Smart windows, mirrors. Although this listing could be subcategorized under the `value-added glass' label, we believe that it is suitably distinct and important to warrant its own heading.

  Typically, the function of a smart window is to electronically block some or all of the light incident onto a window, thereby providing either privacy, if the window is rendered translucent, or control of room lighting and/or temperature (Bonsor 2006). In the latter mode of operation, a smart window eliminates the need for blinds or drapes, and, if UV is blocked, helps to protect carpeting and furniture from fading.

  A smart mirror offers automatic dimming capability, which is useful for trucks, automobiles, ambulances, boats, aircraft, or for homes and buildings. Since closed-loop feedback control using sensors – e.g., solar cells for irradiance and/or thermal couples or alternative technologies for temperature - is desirable for many smart window and mirror applications, there appear to be many possible transparent electronics insertion venues involving control, switching, sensing, etc.

- Transparent solar cells. The idea here is to transmit visible light and to absorb ultraviolet light, converting it into electricity. Accordingly, this is one specific realization of the UV energy harvesting windows previously alluded to in the value-added glass discussion.

Since most of the energy generated in a conventional opaque solar cell is extracted from the infrared and visible portions of the solar spectrum, efficient power conversion of the incident solar irradiance is not a primary objective here. For example, the ideal, theoretical solar cell efficiency of a material with a bandgap of 3.1 eV, i.e., at the visible-ultraviolet transition, is 2.5%, compared to 31% for a maximum efficiency solar absorber material with an optimal bandgap of 1.3 eV (Sze and Ng 2007). Thus, the job of a transparent solar cell would be to scavenge solar energy from the superfluous (and perhaps undesirable) portion of the solar spectrum, so that this energy could be converted to electricity, stored, conditioned, and used in the context of an independent power supply for a more complex stand-alone transparent or partially transparent system.

Possible transparent solar cell device types include pn & pin homojunctions (unlikely, since wide band gap transparent materials are typically unipolar), pn & pin single or double heterojunctions, 'metal'-semiconductor junctions, or 'metal'-insulator-semiconductor junctions (Archer and Hill 2001).

A key question with respect to this application would involve whether the capital investment required to fabricate a transparent solar cell would actually warrant its realization, in terms of system functionality and/or energy payback.

- Reduced-size hard copy unit. Most printer-scanner-copier hard copy systems are relatively bulky, due, in part, to the internal optical source employed, which is typically mechanically translated across the page to be scanned. One way to reduce this bulk would be to integrate a 2-D array of light sources directly onto a glass substrate. This could significantly reduce the size of the system. The solid-state nature of such a system would also lead to an improvement in reliability. The viability of this application depends critically upon the availability, performance, and reliability of the light source arrays.

- Transparent electronics on opaque substrates. Usually, when we conceive of a transparent product, we think of full transparency, such as achieved when we look though a glass window. However, there is no reason to limit transparent applications in this respect, since transparent coatings may be applied directly onto an opaque surface, or indirectly onto a transparent substrate located above the opaque surface, in order to achieve some sort of actuator, sensor, or control functionality. Thus,

the coating would be a surreptitious component of the opaque substrate. Suitable opaque substrates include walls, doors, posts, mirrors, floors, and ceilings. Sound-, motion-, or touch-activation could be used to display reconfigurable information related to advertising, safety, security, directions, etc.

- Transparent circuit boards. Conceive of a set of transparent or partially circuit boards stacked together in a parallel fashion. If intelligent use is made of transparent interconnects and transparent electronics on each circuit board, it is possible that optical signals may be efficiently routed between a large number of circuit boards placed in parallel, thereby to a certain extent circumventing the interconnection bottleneck problem inherent when connecting devices and circuits using conventional opaque wiring schemes. Optical signals could in principle be sent in a perpendicular fashion between glass circuit boards, but also could be waveguided laterally into desired regions of each circuit board. Thus, the routing ability of a circuit board would be enhanced.

The following applications differ somewhat from those just discussed, as they are more generic, in the sense that they involve general application categories, rather than specific application solutions.

- Optometric applications. Visible transparency affords new oportunities in a wide variety of optometric products including eyeglasses, contact lenses, or cornea implants. Futuristic applications might include eyeglasses with communication and display functionality or correctional devices with magnifying and self-focussing capabilities. As with many transparent electronics applications, most optometric `killer apps' will require integration with power sources, sensors, displays, processors, etc. Thus, in these and many other of the applications listed herein, transparent electronics should be viewed as an enabling, ancillary technology, not as a technology providing a complete, drop-in solution.

- X-ray imaging. Amorphous silicon (a-Si)-based large-area image sensor arrays are attractive for x-ray medical or non-medical applications, since x-ray images can be obtained, processed, transferred, and stored electronically, thereby obviating the need for x-ray film (Street 1999; den Boer 2005).

  There are two main x-ray detector array commercial approaches, involving either a photoconductor or a scintillator. In either case,

imaging is accomplished using active-matrix addressing of a two-dimensional array of a-Si TFT switches. In the photoconductor realization, each a-Si TFT is connected to an x-ray photoconductor and a storage capacitor. The x-ray intensity at each pixel node is deduced from the current generated in the x-ray photoconductor which is stored as charge on the storage capacitor. In the scintillator version, the x-ray signal is converted into visible light via the scintillator, which is subseqently detected at each node using an a-Si pin photodiode.

It is not necessary to delve into further technology details, since our purpose here is to simply point out that a transparent electronics backplane may offer advantages compared to that of an a-Si backplane for x-ray imaging applications. These advantages include higher channel mobility, superior device stability, simpler device processing, and visible transparency, which would eliminate the need for light shielding. Active-matrix addressing and these types of potential advantages of transparent electronics compared to a-Si technology are discussed in more detail in Sections 6.3.4 and 6.3.5.

This x-ray imaging application would involve local rather than global transparency.

- Security applications. If you can't easily see it, you probably won't know that it is there, so that it is less likely to be detected. This is a highly desirable attribute from a security perspective. It is not yet clear how this advantage will be reduced to practice in actual applications. `Half-baked` ideas along these lines include invisible UV cameras or detector arrays and transparent radio frequency identification (RFID) tags.

- Automotive applications. An automobile affords numerous application venues for transparent electronics. Obvious candidate platforms include window glass, dashboards, and navigation systems. It is likely that transparent electronics will constitute an ancillary technology for most of these applications, requiring integration with a display, sensor, actuator, etc. in order to meet the overall subsystem requirement.

- Military and aerospace applications. Based on the number of military persons who have contacted us about our transparent electronics work and the interest engendered in our participation in a military electronics conference (Wager et al. 2003), we are confident that a mature

transparent electronics technology will lead to many military and aerospace applications. Some of these applications will be identical to those found in the commercial sector, e.g., transparent displays. However, it is likely that other more specialized applications involving, for example, command, communication, and control, security, or display functionality, will emerge.

- Toys, games, art. Some of the most creative uses of cutting-edge, `high-tech' are found in toys, games, and artistic creations. Innovators in this arena are much too imaginative to allow us to accurately predict or anticipate their future directions. However, we believe that the inherent novelty of transparent electronics naturally lends itself in this direction. Again, we have already received some very interesting calls and emails confirming this to be the case.

3.4 Applications in retrospective

Many different obvious and perhaps not so obvious transparent electronics application possibilities have been considered in this chapter. Which ones are the 'killer apps' for which we are all searching? Again, our crystal ball is a bit fuzzy when confronted with this query. Therefore, perhaps we now need to roll up our sleeves and continue working towards the realization, optimization, and elucidation of the many types of materials, devices, circuits, and systems that will eventually constitute this new, emerging technology.

4 Materials

4.1 Device components

The realization of a viable transparent electronics technology is critically dependent on the availability of materials and processes that will lead to the production of robust devices at reasonable cost. In this chapter, we discuss the various types of materials that are envisioned for these applications.

The fabrication of active devices requires the deposition of thin films having appropriate properties to function as high-performance channel materials, transparent metals, and dielectrics. Because the visible region extends from 400 to 700 nm, it is commonly accepted that all of the materials should have band gaps $\geq$ 3.1 eV. As noted in Chapters 1 and 2, and discussed in more depth in Chapter 5, a high majority carrier mobility and a minimal carrier concentration consistent with trap filling are desirable characteristics for a channel semiconductor. Similar materials with high carrier concentrations can be optimized to produce useful transparent conductors. Because active transparent devices are being produced on a variety of substrates, a native oxide such as SiO_2 in silicon electronics is not available as a dielectric. In many ways, the optimization of the gate dielectric in a TTFT mirrors that of the high-k approaches under development in advanced silicon CMOS technologies (Robertson 2006).

In this chapter, we primarily consider the materials characteristics of semiconductor materials in TTFTs. Insulator development for gate dielectrics in TTFTs is an expanding topic, and recent developments are noted. The performance of transparent conductors is already approaching proposed theoretical limits, and their properties have been extensively considered elsewhere (Gordon 2000).

4.2 n-type semiconductor channel materials

As noted in Chapter 1, ZnO, In_2O_3, and SnO_2 are the three primary polycrystalline materials serving as channel layers in transparent transistors. Each of these semiconductors is transparent throughout the visible portion of the electromagnetic spectrum with a band gap that is positioned in the near ultraviolet. Despite their large gaps, these materials can be processed with native or extrinsic defects that contribute to the creation of free carriers and a positioning of the Fermi level near or within the conduction band. The placement of the Fermi level inside the conduction band might be expected to lead to optical absorption with transitions from the Fermi level into empty conduction band states, rendering the materials opaque. Even at high carrier concentrations, however, visible transparency is not severely limited. The crystal and electronic structures as well as the defect chemistries of these materials and their derivative compositions play major roles in affecting the salient optical and electrical properties that contribute to the successful use of these and derivative compounds in transparent electronics.

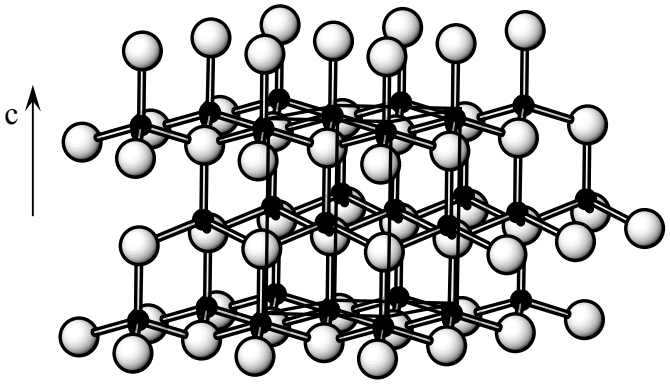

Fig. 4.1 Hexagonal structure of wurtzite. Zn – small, filled spheres; O – large shaded spheres.

Under common synthesis conditions, ZnO adopts the hexagonal wurtzite structure (Fig. 4.1). The structure is commonly described as a slightly distorted hexagonal closest packing of O atoms with Zn atoms occupying half of the available interstitial distorted tetrahedral sites. The net result is a fourfold coordination of Zn by O (and of O by Zn) and a three-

dimensional framework of vertex-sharing ZnO_4 (or OZn_4) tetrahedra. As seen in Fig. 4.1, three of the O atoms in the distorted ZnO_4 tetrahedron are placed in one close-packed *ab* plane, while the fourth O atom is located in an adjacent plane. As a result, the structure contains an array of vertical Zn-O vectors along the *c* axis, resulting in a classical polar structure. Other structural forms of ZnO are much less studied, but the cubic zincblende form has been stabilized by deposition of thin films on cubic substrates (Ashrafi et al 2000). The rocksalt structure has been synthesized in bulk by using high-pressure techniques (Bates et al 1962; Gerward and Olsen 1995; Recio et al 1998) and in films by doping with Mg (Haruki et al 2006; Vashaei et al 2006). In all reported ZnO TTFTs, ZnO adopts the wurtzite structure.

As seen in Fig. 4.2, In_2O_3 crystallizes in the structure of the cubic mineral bixbyite $(Fe,Mn)_2O_3$. This structure is often described as a derivative of fluorite CaF_2, where ¼ of the anions are removed followed by a slight shifting of the atoms. The net result is a dense three-dimensional structure of InO_6 octahedra sharing edges. The In atoms occupy two crystallographically distinct InO_6 environments; in one environment, the six O neighbors are equidistant at 2.18 Å, while in the other two O atoms are located each at 2.13, 2.19, and 2.23 Å. The O atoms occupy highly distorted tetrahedral environments with In-O-In angles ranging from 100 to 126°.

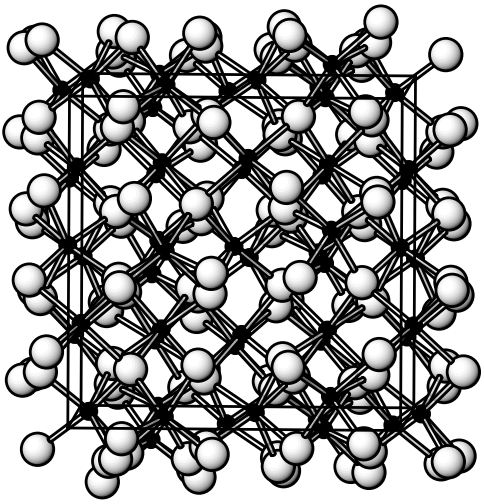

Fig. 4.2. Structure of cubic In_2O_3. In – small filled spheres; O – large shaded spheres.

Like many binary metal oxides with the stoichiometry MO_2 and polar M-O interactions, SnO_2 crystallizes in the tetragonal rutile structure, *cf*., Fig. 4.3. In this structure, the O atoms adopt a highly distorted version of hexagonal closest packing. The Sn atoms occupy one-half of the available octahedral interstices, leaving the O atoms with a coordination number of three. The parallel chains of edge-shared SnO_6 octahedra extending along the *c* axis distinguish the rutile structure. These chains are fused into the full three-dimensional framework by sharing O atoms, which are themselves bound to three Sn atoms in a triangular fashion.

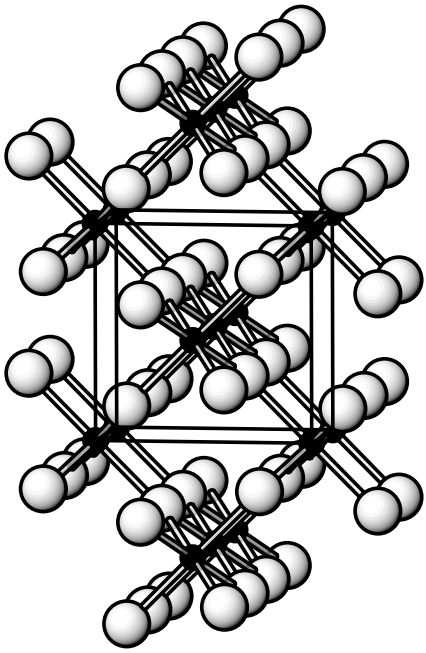

Fig. 4.3. View of the tetragonal structure of SnO_2 along the *c* axis. Sn – small filled circles; O – large open circles.

In comparing the properties of ZnO, In_2O_3, and SnO_2, it is useful to consider the metal-atom number densities and associated metal-metal distances. As seen in Table 4.1, as the metal:oxygen ratio decreases across the series ZnO → In_2O_3 → SnO_2, the number density decreases by approximately 25% and the metal-metal distances increase by approximately 14%. As described below, the electrical properties of these materials are dominated by the 4*s* orbital of Zn and the 5*s* orbitals of In and Sn. While the larger radial extension of the 5*s* orbital relative to the 4*s* orbital might be expected to lead to higher mobilities and conductivities for In_2O_3 and

SnO_2, the higher number densities and shorter metal-metal distances in ZnO lead to largely equivalent properties for all three materials.

Table 4.1. Structural characteristics of oxide semiconductors.

Semiconductor	Metal number density (cm^{-3})	Metal-metal distances (Å)
ZnO	3.8×10^{22}	3.21, 3.24
In_2O_3	3.1×10^{22}	3.36, 3.83
SnO_2	2.8×10^{22}	3.71

Considerable effort has been devoted to developing an understanding of the electronic structures (Woodward et al. 2006) and defect chemistries that contribute to the unusual physical properties of ZnO, In_2O_3, and SnO_2. While many aspects of the features of these materials require additional detailed study, the current level of understanding does provide useful working models and guidelines for device studies and the development of new materials and processes for enhanced performance.

ZnO, In_2O_3, and SnO_2 are simple valence compounds containing metal ions with ns^0 and oxide anions with $2s^2 2p^6$ valence electron configurations. These levels give rise to the schematic energy-level diagram depicted in Fig. 4.4, which is applicable to all three compounds. In ideally stoichiometric materials, the Fermi level is associated with filled O $2p^6$

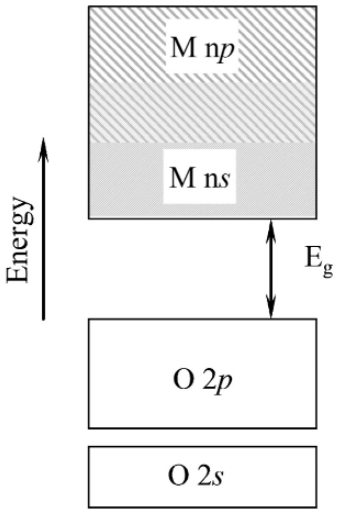

Fig. 4.4. Schematic energy-level diagram for ZnO, In_2O_3, and SnO_2.

valence bands (VBs) and empty metal-centered ns^0 conduction bands (CBs). Real samples, however, contain intrinsic or extrinsic defects that contribute to the production of charge carriers and placement of the Fermi level near or within the n*s* conduction band, producing *n*-type transport characteristics. Among the three materials, ZnO is unique in exhibiting identifiable, narrow Zn 3d bands several eV below the top of the VB. In considering band structures for these materials, it is worthwhile to note that there is insignificant n*s*-n*p* orbital mixing at the Γ point. Moving away from this point, the *s*-band exhibits greater mixing with the *p* orbitals, a high dispersion, and an approximately parabolic shape characteristic of the free-electron model for a metal. The high dispersion of the band contributes to a small electron mass (~0.3 m_e) (Young et al 2000) and a high mobility. The large energetic separation between the bottom of the n*s* conduction band and the higher lying n*p* bands contributes to the maintenance of transparency, despite the significant electron occupation of the conduction band in the degenerate state. From a chemical perspective, the materials exhibit highly polar covalent M-O interactions, consistent with the observed band gaps and the O-centered character of the valence band and the metal-centered character of the conduction band. As such, *p*-type doping relying on hole generation in narrow O *p* bands is problematic, especially in terms of achieving significant carrier concentrations and high conductivities.

Under metal-rich, O-deficient growth conditions at high temperatures, free-carrier densities can be adjusted through the range of $10^{17} – 10^{20}$ cm^{-3} with O deficiencies commonly up to 1 at% (de Wit 1975; de Wit et al. 1976; Halliburton et al. 2005; Nakazawa et al. 2006); further extrinsic doping can produce densities in the range of 10^{21} cm^{-3}. The materials exhibit a paradoxical coexistence of coloration characteristic of insulators containing deep defect centers and conductivities and carrier concentrations indicative of shallow centers. For ZnO, the most commonly considered defect centers are O vacancies (V_O), Zn occupying interstitial sites (Zn_i), and H occupying interstitial sites (H_i). H_i has been found both experimentally and theoretically to be a shallow donor in ZnO, contributing to high carrier concentrations (Van de Walle 2000). In annealed materials, however, where H concentrations are reduced, elevated carrier concentrations can still be observed. Zn_i has commonly been implicated as a donor, but recent calculations indicate that its formation energy is too high to produce a concentration sufficient to account for the observed carrier concentrations. As noted above, ZnO has often been often characterized by a significant V_O concentration. Modeling studies also reveal V_O is the most abundant de-

fect, and its concentration is found to be quite similar to the carrier concentrations observed in single crystals (Lany and Zunger 2005). Like other wide-gap oxides, the neutral vacancy, V_O^0, however, is predicted to function as a deep level, which should only contribute to sample coloration through the optical excitations of the type $V_O^0 \rightarrow V_O^+ + e$ and $V_O^+ \rightarrow V_O^{2+} + e$. These excitations also contribute to a persistent photoconductivity and to the observed conducting nature of the material through electron population of the conduction band.

Electrical conduction in SnO_2 is correlated with nonstoichiometry. Resistive samples can be produced (Terrier et al. 1995), and conductivity increases by orders of magnitude through control of oxygen partial pressure and V_O concentrations during deposition and processing (Chopra et al. 1983). Like ZnO, V_O in SnO_2 is expected to form a deep center. In modeling studies, however, interstitial Sn_i has been found to produce donor levels inside the conduction band (Kilic and Zunger 2002); its formation energy is calculated to be sufficiently low to produce high concentrations and significant conductivities. In fact, a synergistic effect has been proposed for the formation of Sn_i and V_O defects. In the structure of SnO_2 (Fig. 4.3), empty channels rimmed by O atoms extend along the *c* axis. Direct placement of Sn_i in the channels produces a local coordination environment (Fig. 4.5) about the Sn_i that is largely indistinguishable from that of the native Sn site. In the presence of an associated V_O, however, structural relaxation is anticipated. The regular coordination is that commonly associated with Sn^{4+}, whereas the relaxed forms mimicks that found in oxides of Sn^{2+}. Hence, the ready ability of Sn to adapt to a relaxed coordination environment appears to play a role in establishing the very high V_O concentrations that can be produced in SnO_2. Such behavior contrasts to insulating oxides such as MgO and SiO_2, where the single oxidation states of Mg and Si do not allow for such relaxation and, by extension, significant interstitial metal concentrations.

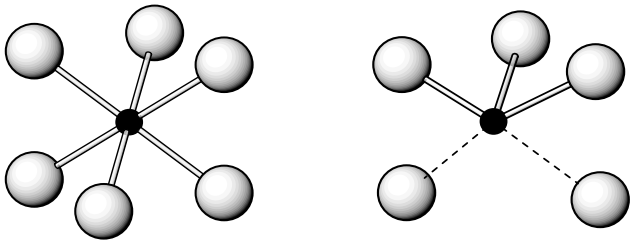

Fig. 4.5. (left) Regular Sn_i environment in SnO_2. (right) Relaxed Sn_i-Vo environment in SnO_2.

The details of the electrical transport properties of ZnO, In_2O_3, and SnO_2 have been determined through Hall-effect measurements on single crystals and epitaxial films. It should be noted, however, that existing TTFTs have been fabricated on the basis of polycrystalline materials. Nevertheless, the single crystal and epitaxial films provide a benchmark in assessing the performance characteristics of corresponding devices.

Resistivity and Hall measurements provide data on carrier type, carrier concentration, and mobility. A four-terminal Van der Pauw measurement can be used to assess the sheet resistance, R_S, of a material, which can be coupled with the sheet carrier concentration, n_S, from a Hall measurement to determine the mobility (μ) via

$$\mu = \frac{1}{qn_S R_S} \tag{4.1}$$

where q is the electron charge. The mobility is the proportionality constant relating the drift velocity to the applied electric field $v_d = \mu E$, and its magnitude is correlated to the scattering mechanism limiting the low drift field velocity. As carriers travel through an oxide semiconductor, they encounter events – impurities, phonon modes, strain, and defects – that affect their mobility. The parameter for characterizing the various scattering mechanisms is the relaxation time τ. Mobility is related to this scattering time by

$$\mu = \frac{q\langle\tau\rangle}{m^*} \tag{4.2}$$

where m* is the electron effective mass, q is the electron charge, and $<\tau>$ is the relaxation time averaged over the energy distribution of the electrons.

By using Monte Carlo simulation, the electron mobility of single-crystal ZnO has been estimated to be 300 $cm^2\ V^{-1}\ s^{-1}$ (Albrecht et al. 1999). From bulk crystals of ZnO grown by a chemical vapor-transport method, a mobility of 205 $cm^2\ V^{-1}\ s^{-1}$ at a carrier concentration of 6 x 10^{16} cm^{-3} has been reported (Look et al. 1998). For epitaxial films grown by PLD and MBE, electron mobilities cover the range 120 - 155 $cm^2\ V^{-1}\ s^{-1}$ with carrier con-

centrations of 0.2 – 7.4 x 10^{16} cm^{-3} (Kaidashev et al. 2003; Miyamoto et al. 2004).

For In_2O_3, a room-temperature mobility of 160 cm^2 V^{-1} s^{-1} with carrier concentration near 10^{18} cm^{-3} has been reported for bulk single crystals grown by a vapor-phase method (Weiher 1962). A mobility of 50 cm^2 V^{-1} s^{-1} has been reported for epitaxial films on YSZ grown via pulsed laser deposition (Tarsa et al. 1993), while mobilities > 100 cm^2 V^{-1} s^{-1} for films doped with Zr and W (Koida et al. 2006; Newhouse et al. 2005).

The mobility of SnO_2 single crystals has been reported to be as high as 200 cm^2 V^{-1} s^{-1} (Nagasawa et al. 1965) with a carrier concentration of 10^{17} cm^{-3}. For epitaxial films deposited by pulsed laser deposition, a mobility of 37 cm^2 V^{-1} s^{-1} at a carrier concentration of 10^{19} cm^{-3} has been observed (Dominguez et al. 2006). Overall, the experimentally observed electron mobilities for ZnO, SnO_2, and In_2O_3 crystals and films are quite similar. Such a result is consistent with the similarities in the conduction-band structures of the materials.

As noted earlier, extremely high carrier concentrations may readily be realized under metal-rich, O-poor growth conditions and by doping with elements whose donor levels are shallow with respect to the conduction band minimum. These degenerate doping conditions, however, differ from those usually encountered in single-crystal and epitaxial semiconductor devices. At higher carrier concentrations, significant ionized impurity scattering occurs in these materials, and mobilities drop considerably. Such high carrier concentrations and scattering correspond to doping levels and properties relevant to TCO applications, *cf.*, Table 1.1. Thus, according to this carrier concentration - ionized impurity scattering - mobility trend, it would be expected that mobilities would remain high in the very low carrier-concentration regime of a TTFT channel layer, where carrier concentrations are intentionally minimized to avoid deleterious conductive channel effects, as discussed in Section 5.3.2. As discussed below, in a polycrystalline semiconductor, at low carrier concentrations the advantages of ionized impurity trends are negated by grain boundary transport considerations, so that the mobilities are not as large as expected on the basis of ionized-impurity-scattering considerations alone.

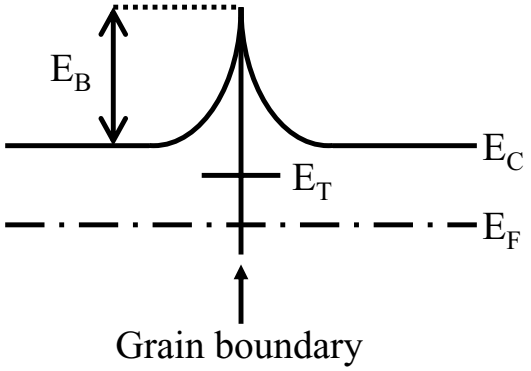

Fig. 4.7. One-dimensional energy band diagram model for an n-type polycrystalline material, where inter-grain electron transport involves surmounting an energy barrier, E_B. E_T denotes the energy of a grain-boundary trap, which is assumed to be discrete and acceptor-like.

Grain boundary transport in polycrystalline materials may be understood (Hartnagel et al. 1995; Hossain et al. 2003; Kuo 2004b) with the aid of an energy band diagram, such as the one given in Fig. 4.7 for an n-type material, where electron transport is operative. The basic idea here is that a grain boundary can be treated as an internal surface that traps charge. If this trapped charge at the grain boundary is modeled as a discrete acceptor trap with energy E_T, as shown in Fig. 4.7, charge neutrality considerations indicate that negative charge trapped at the grain boundary, qN_{GB}, will be balanced by positive charge associated with donor doping, qN_D, in the depletion region surrounding the grain boundary, thereby giving rise to an energy barrier, E_B. Thus, the boundary can be considered to be a back-to-back Schottky barrier from an inter-grain transport perspective. Electron transport between grains will be inhibited by the energy barrier indicated as E_B in Fig. 4.7, which at large donor doping densities may be approximated as

$$E_B \approx \frac{q^2 N_{GB}^{\ 2}}{8\varepsilon_S N_D}. \tag{4.3}$$

Electron transport in a polycrystalline material which is dominated by inter-grain transit involving thermionic emission over the energy barrier E_B may be modeled as

$$\mu_{GB} = \mu_o e^{\frac{-E_B}{k_B T}}, \tag{4.4}$$

where μ_o is the zero-barrier mobility. The overall bulk mobility in a polycrystalline material, μ, is obtained from summing in an inverse fashion the single grain mobility, μ_G, and the grain boundary mobility, μ_{GB}, as follows

$$\mu^{-1} = \mu_G{}^{-1} + \mu_{GB}{}^{-1}. \tag{4.5}$$

Within the context of Eqs. 4.3-5, consider the effect of increasing the donor doping density on the mobility. For low doping densities, E_B is large so that μ is small because electrons within a grain cannot surmount the inter-grain energy barrier. As the doping density increases, the E_B decreases so that μ, which is still dominated by grain boundary barrier-inhibited transport, will increase. However, once E_B is negligibly small, μ will decrease with increasing doping density since ionized impurity scattering begins to dominate.

This grain boundary inhibited transport in polycrystalline materials has important TTFT implications. When binary oxides such as ZnO, In_2O_3, or SnO_2 are employed as TTFT channel materials, they invariably are nanocrystalline. Such semiconductor materials with a high density of grain boundaries will function as channel layers in TTFTs because these films are highly insulating as a consequence of overlapping, grain boundary-induced depletion regions. However, the severe price paid is that the channel mobility is inherently poor relative to that observed in single crystals and epitaxial films because of the dominance of grain boundary inhibited transport.

4.3 Amorphous oxide semiconductors

As just discussed, in polycrystalline materials, grain boundaries play a major role in determining a variety of performance characteristics in active electronic devices. Amorphous materials provide a means to eliminate the effects of these boundaries, especially for devices covering large areas. Of course, amorphous Si (*a*-Si) with its use in active-matrix flat-panel displays is the preeminent example of the control obtained with an amorphous semiconductor.

Like *a*-Si, amorphous oxide semiconductors (AOS) have been known for more than 50 years (Denton et al. 1954). Early work was directed to the preparation and study of a variety of glassy transition-metal oxides, largely dominated by compositions rich in V_2O_5. These materials exhibit conductivity on the basis of variable-range hopping with mobilities on the order of only 10^{-4} cm^2 V^{-1} s^{-1} (Mori et al 2000), values much too low for practical applications. Because of the presence of the transition metals, these films are also quite highly colored, preventing their use in transparent electronics. One of the early studies of transparent amorphous semiconductors was directed to an examination of the amorphous-to-crystalline phase transition of In_2O_3 thin films prepared by reactive evaporation (Ito et al. 1987). Later, detailed analyses of the electrical and optical properties were undertaken with amorphous In_2O_3 films deposited via ion-beam sputtering (Bellingham et al. 1991). These films exhibited carrier concentrations near 10^{20}/cm^3 and resistivities near 10^{-4} Ω cm - these values are comparable to those achieved with crystalline films, indicating that ionized impurity scattering is the dominant factor in limiting electron mean-free paths and conductivities when these materials are heavily doped such that grain boundary barriers are of negligible importance.

The results deduced from In_2O_3 developmental studies sparked a more general consideration of AOSs through studies of Cd_2GeO_4 (Hosono et al. 1995; Kikuchi et al. 1997), $AgSbO_3$ (Yasukawa et al. 1995; Yasukawa et al. 1996), and $InGaZnO_4$ (Orita 2001). Many of the properties of these materials can be demonstrated by consideration of Cd_2GeO_4. The amorphous structure of this material in thin-film form has been confirmed by XRD measurements and TEM observations. Films are optically transparent (E_g = 3.4 eV) and electrically insulating ($\sigma_{300\,K} = 10^{-9}$ S cm^{-1}), although conductivity can be increased by 11 orders of magnitude to 10^2 S cm^{-1} by ion implantation of appropriate cations such as H^+ and Ti^+. The activation energy of the electrical conductivity continuously decreases from 1.1 to ~0 eV as the implanted dose increases, indicating that the Fermi level is controllable from deep in the bandgap to above the conduction band minimum. The Hall mobility in the degenerate state (carrier concentration: ~10^{20} cm^{-3}) is 10-12 cm^2 V^{-1} s^{-1}, which is only slightly smaller than that (~15 cm^2 V^{-1}s^{-1}) in polycrystalline Cd_2GeO_4.

Free carrier absorption appearing in the infrared region can be described by a simple Drude formula. The effective mass is evaluated as 0.33 m_e, which agrees with that estimated from the Burstein-Moss shift (band gap widening due to electron filling above the CBM), and the mean free path

of the electron is more than an order of magnitude larger than the chemical bond length.

The nature of the CBM was examined by combining photoelectron spectroscopy with calculations of the structural model determined from the radial distribution function assisted by reverse Monte-Carlo simulation (Narushima et al. 2002). The CBM is found to be primarily composed of Cd 5*s* orbitals with a considerably smaller contribution from Ge 4*s* levels. These results are consistent with a simple model involving Cd 5*s* orbitals as the main contributors to the electrical conductivity with Ge serving a role to promote the formation of the amorphous structure by preventing the crystallization of CdO. Considering the spherical nature of the Cd *s* orbitals, their overlap is only modestly affected by the specific nature of the ordering in the structure, i.e., whether it is crystalline or amorphous. As schematically indicated in Fig. 4.8, despite the loss of structural periodicity and dilution of active *s* orbitals resulting from the inclusion of metal atoms that do not contribute to the conduction-band minimum, pathways for electrical conduction are maintained in the amorphous phase. As a result, the transport properties of the amorphous and crystalline phases are much more similar than typically observed when comparing the properties of amorphous and crystalline phases of other elemental and compound semiconductors.

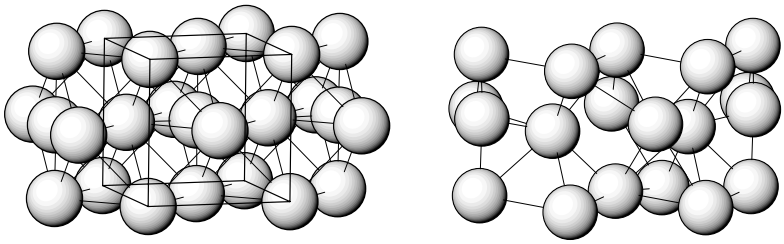

Fig. 4.8. Representations of s-orbital arrays contributing to conduction band minima in (left) a crystalline oxide semiconductor and (right) an amorphous oxide semiconductor.

Recently, the structure of amorphous IGZO has been modeled by using computational simulations in conjunction with EXAFS (Nomura et al. 2007), which is a useful X-ray absorption technique for determining short-range structural features. The average coordination numbers of the In, Ga, and Zn atoms by O atoms have been determined to be >5, ~5, and ~4, re-

spectively. The coordination number of In, representing a mixture of 5- and 6-coordinate sites, is a distinguishing feature of *a*-IGZO, as single crystalline IGZO contains only 6-coordinate In atoms. This difference in coordination number between the amorphous and crystalline phases has been proposed as one contributor to the 5% decrease in the density of the amorphous phase relative to the crystalline material. In the modeling studies, however, a higher proportion of vertex-sharing polyhedra is proposed for the amorphous phase, which also should lead to larger volumes and lower densities. Band-structure calculations for an optimized amorphous structure reveal no localized states in the vicinity of the conduction band and large overlap between the In 5*s* orbitals. Presumably, Zn 4*s* orbitals also contribute to the bottom of the conduction band, since IGZO materials rich in Zn exhibit relatively high mobilities.

Transparent AOSs share several properties that are generally not observed in conventional amorphous semiconductors. Electron mobilities ($10 - 40$ cm^2 V^{-1} s^{-1}) in devices are relatively high, exceeding *a*-Si by a factor > 10 and most organics by a factor > 10^2. In contrast to other amorphous semiconductors, highly conducting degenerate states can be realized by doping. While crystalline Si can readily be doped to produce degenerate behavior, such a state can not be produced with *a*-Si. In conventional amorphous semiconductors, conduction takes place by hopping between tail sates, producing mobilities in the amorphous materials that are considerably lower than those of the crystalline state. In contrast, with appropriate doping or via gate voltage control in a TTFT, the Fermi level can be located in the conduction band of an AOS, resulting in degenerate behavior consistent with band conduction. As noted for the crystalline oxide semiconductors, carrier concentrations can be controlled through oxygen vacancy concentrations. Thus, an effective way to control oxygen concentrations in AOSs is by adjusting the oxygen vapor pressure during deposition and post-deposition processing. In this way the valence states of the *n*s metals can be manipulated, charge can be injected into the CBM, and trap states can be filled.

A study on the system ZnO-SnO_2, which is largely amorphous, exemplifies some of these processes (Hoffmann 2006). Here, TTFT turn-on voltages, V_{on}, and incremental mobilities, μ_{inc}, were measured as a function of composition (Zn:Sn ratio) and process temperature. Consistent with many other observations (Presley et al 2006) and the demonstrated propensity for O-vacancy formation, TTFTs with SnO_2 as the channel material could not be turned off. Similarly, the Sn-rich composition Zn:Sn of 1:2 exhibits a

precipitous drop in V_{on} to negative values between 300 and 500 ^{o}C, although between 500 and 600 ^{o}C the value exhibits a positive slope. For compositions richer in Zn, V_{on} exhibits a steady decrease from positive to negative values with increasing temperature, resting near zero at 400 ^{o}C. For the intermediate Zn:Sn ratios, sharp increases in μ_{inc} are observed for annealing temperatures between 200 and 400 ^{o}C, which track the decreases in V_{on} over the same temperature range. These changes in device operation are related to the underlying material alterations occurring under the various processing conditions. The decreases in V_{on} and associated increases in μ_{inc} are associated with trap filling and higher concentrations of free electrons at a given gate voltage that contribute to the formation of a conducting channel. Considering these results and compositional variations, the formation of O vacancies, especially at higher temperatures, clearly plays a major role in establishing the observed trends. The nature of long-range *vs.* short-range structural ordering as well as other temperature-dependent effects contributing to defect formation and annihilation will contribute to the interrelationships between materials properties and device performance.

4.4 p-type semiconductors

4.4.1 Copper oxides and chalcogenides

To complement the applications and performance characteristics of the *n*-type oxides in extending the capabilities of transparent electronics, efforts have been directed to the development of useful *p*-type wide band-gap semiconductors. While numerous crystalline and amorphous *n*-type transparent semiconductors can readily be produced on the basis of the occupation of *n*s-orbital bands in metal oxides, only a few transparent *p*-type semiconductors are known, and they are exemplified by oxides and chalcogenides of copper. Here, the $d^{10}s^{0}$ electron configuration of Cu(I) provides a large band gap and the means for introduction of holes through partial oxidation of Cu(I).

A schematic energy-level diagram applicable to Cu(I) oxides and chalcogenides is illustrated in Fig. 4.9. The upper portion of the valence band is characterized by Cu 3*d* –X n*p* (X = O, S, Se, Te) interactions. These interactions give rise to bands that are bonding at lower energies and antibonding at the higher energies corresponding to the top of the valence

band. These bands are energetically separated from the higher lying Cu 4*s* levels, which characterize the bottom of the conduction band. In many ternary compounds, the resulting band gap occurs near 3 eV or higher, providing transparency across the visible spectrum. Because Cu(I) can be readily oxidized to Cu(II), holes, for example, as Cu vacancies can be easily introduced into the valence band to produce *p*-type conductivity. The presence of these vacancies and the need for charge compensation results

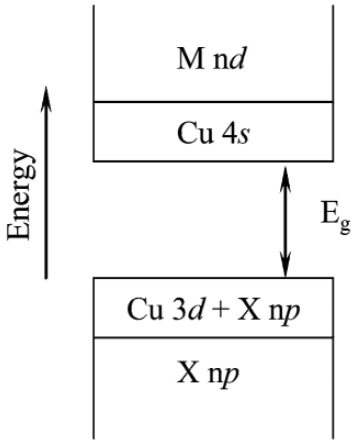

Fig. 4.9. Schematic energy-level structure for a ternary MCuQX compound (M = lanthanide, alkali metal, or alkaline-earth metal; Q = O, S, Se, Te).

in the formal formation of d^9, Cu(II) centers and the introduction of holes in the valence band. The process is equivalent, but of opposite polarity, to the introduction of electron carriers through native O vacancies in the n-type oxides of Zn, In, and Sn. In contrast to the *s*-orbital *n*-type oxides, the conduction path for the copper compounds involves a stronger mixture of Cu *d* and anion *p* orbitals. Given the contracted nature and directional characteristics of the *d* orbitals relative to the *s* orbital, flatter bands and smaller carrier mobilities should be anticipated.

The inception of efforts to realize wide band-gap *p*-type oxides is generally attributed to the initial report on $CuAlO_2$ (Kawazoe et al. 1997), which exhibits a band gap > 3 eV. The oxide was deposited in polycrystalline form via pulsed laser processing, and resulting films were reported to exhibit a positive Seebeck coefficient (+183 $\mu V\ K^{-1}$) characteristic of *p*-type carriers, conductivity of 1 $S\ cm^{-1}$, and a carrier mobility near 10 $cm^2\ V^{-1}\ s^{-1}$. These initial findings were very promising, indicating that transparent *p*-type oxides with performance characteristics comparable to those of their

n-type counterparts could be realized. Unfortunately, these data, especially the high mobility, have not been reliably reproduced, and attempts to increase carrier concentrations in the material have proven unsuccessful. As a result, the initial promise of $CuAlO_2$ has not been realized. The early work on the material, however, did stimulate research on the related compounds $CuMO_2$ (M = Ga, In, Sc, Y, La) (Duan et al. 2000; Jayraj et al. 2001; Kykyneshi et al. 2004; Yanagi et al. 2001), which like $CuAlO_2$ crystallize in the delafossite structure (Fig. 4.10).

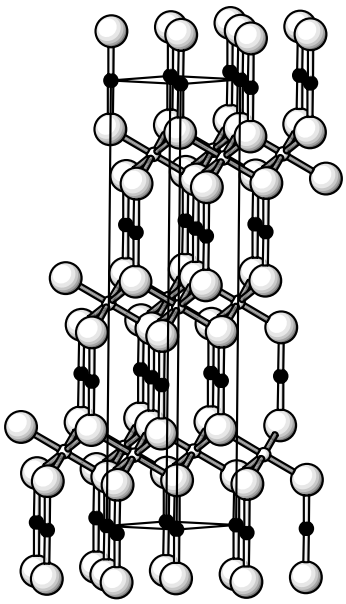

Fig. 4.10. Crystal structure of the delafossite phase $CuMO_2$ (M = +3 cation); Cu – small filled circles, M – small open circles, O – large open circles.

In the delafossite structure, layers of M-centered O octahedra are bridged by linear sticks of O-Cu-O that are oriented parallel to the *c* axis, *cf.*, Fig. 4.10. It is important to note that these sticks are essentially isolated, producing no -Cu-O-Cu- linkages; the Cu···Cu separation is also relatively long. These features produce a flat valence band that exhibits partial Cu *d*-orbital character. In those structures with large M atoms, e.g., In, Y, and La, it is possible to insert additional O atoms into the structure by carefully heating samples in air. These O atoms occupy sites between the Cu atoms in the Cu planes, providing -Cu-O-Cu- linkages. During the initial stages of this O insertion process, Cu(I) atoms becomes locally oxi-

dized, resulting in the formation of isolated Cu(II) atoms, an intense coloration of the samples, and only limited improvement in conductivity. At higher O loadings, more extensive -Cu-O-Cu- linkages are formed and conductivities increase, but the resulting samples are now opaque and of limited value for transparent electronics.

The ternary copper oxide $SrCu_2O_2$ has also been examined as a transparent conductor (Kudo et al. 1998). This material exhibits a band gap of 3.3 eV with *p*-type carriers confirmed by Seebeck and Hall measurements on thin films prepared via pulsed laser deposition. Relative to the delafossite compounds, the structure (Fig. 4.11) would appear to be more conducive to high carrier mobilities. Zig-zag chains of -Cu-O-Cu- linkages extend along the *a* axis of the tetragonal cell, providing a conduction path for holes. The structure also produces a relatively short Cu···Cu distance, 2.74 Å.

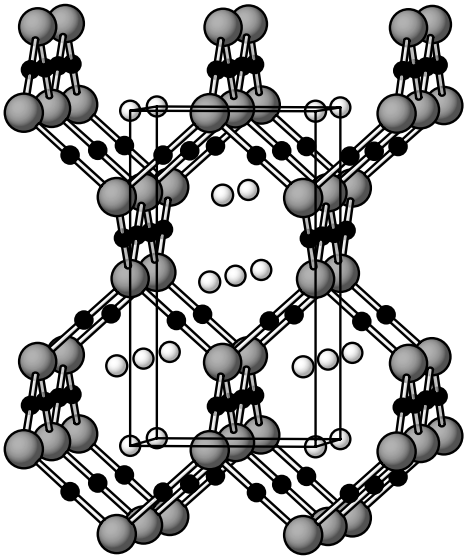

Fig. 4.11. Crystal structure of $SrCu_2O_2$. Sr – small open spheres, Cu – small black spheres, O – large gray spheres.

The electronic structure of $SrCu_2O_2$ is related to that of Cu_2O. The valence band maximum is comprised of Cu 3*d* and 4*s, p,* and O 2*p* orbitals, while the conduction band minimum is comprised of Cu 4*s, p,* and O 2*p* orbitals (Ohta et al. 2002; Boudin et al. 2003; Lynch et al. 2005). Un-

doped and K-doped polycrystalline films grown by pulsed laser deposition have conductivities of 3.9 x 10^{-3} and 4.8 x 10^{-2} S cm^{-1}, respectively. For the K-doped film, the Seebeck coefficient is +260 μV K^{-1}, the carrier concentration is 6 x 10^{17} cm^{-3}, and the mobility is 0.5 cm^2 V^{-1} s^{-1}. The temperature dependence of the conductivity reveals a thermally activated process with an activation energy of 0.1 eV. TTFT device operation with a channel layer of $SrCu_2O_2$ has not been reported; optoelectronic devices, however, have been described in Section 2.1.

The oxide chalcogenides (LnCuOQ; Ln = lanthanide, Q = S, Se, Te) and fluoride chalcogenides (MCuFQ; M = Ba, Sr, Ca) represent additional families of wide band-gap Cu-based semiconductors. These materials all adopt a layered structure (Fig. 4.12), wherein edge-shared CuS_4 tetrahedra form sheets in the *ab* plane that are widely separated by [LnO] or [MF] layers. These structural features are expected to impart a strong anisotropic character to the transport properties, as carrier transport is confined to the two-dimensional Cu-Q sheets.

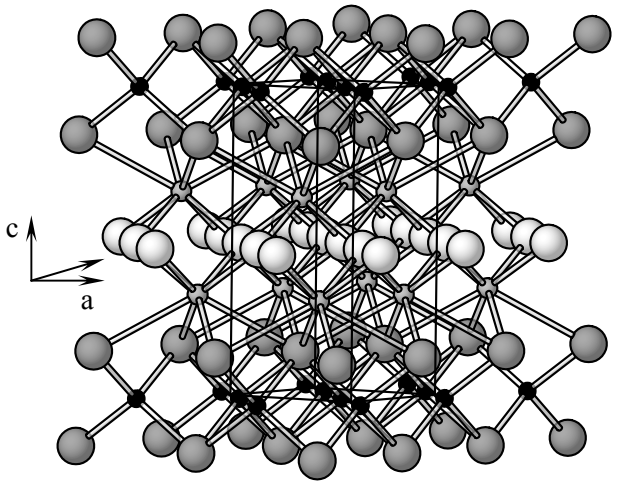

Fig. 4.12. Crystal structure of LnCuOQ and MCuFQ. Ln,M – small gray spheres; Cu – small black spheres; O, F – large open spheres; Q – large gray spheres.

The band gaps of LaCuOS and LaCuOSe are 3.1 and 2.7 eV, respectively. Each undoped material exhibits activated semiconductor conductivity; substitution of approximately 3% Sr for the La in sintered pellets leads to an increase in conductivity from approximately 10^{-4} to 10 S cm^{-1} and degenerate behavior (Ueda et al. 2006). Epitaxial (001)-oriented films

for the series $LaCuOS_{1-x}Se_x$ ($0 \leq x \leq 1$) have been grown via pulsed laser deposition on MgO substrates (Hiramatsu et al. 2002). On the basis of Seebeck measurements, all of the films are *p*-type. The sulfide exhibits a conductivity < 1 S cm^{-1} and mobility < 1 cm^2 V^{-1} s^{-1} with carrier concentration near 10^{19} cm^{-3}, while the selenide exhibits a conductivity of 20 S cm^{-1} and mobility near 8 cm^2 V^{-1} s^{-1} at a similar carrier concentration. For the selenide, Mg doping leads to an increase of the carrier concentration to 10^{20} cm^{-3} and a conductivity as high as 140 S cm^{-1}.

Similar observations have been made for the compounds BaCuSF and BaCuSeF, which have band gaps of 3.2 and 2.9 eV, respectively (Park et al. 2003). K substitution, for example, leads to conductivities of order 10^2 in pressed pellets. Because of the loss of K during deposition, however, these results have yet to be reproduced in thin films. Pulsed laser deposition of BaCuTeF on MgO substrates between 500 and 650 ^oC results in *c*-axis oriented films. Deposition of thin films in a background of 1 mTorr Ar leads to a *p*-type conductivity of 167 S/cm with a carrier concentration of 10^{20} cm^{-3} and mobility of 8 cm^2 $V^{-1}s^{-1}$. Curiously, while a small absorption onset is observed for the films near 2.3 eV, the strongest absorption feature occurs at energies near 3 eV.

4.4.2 Rhodium oxides

To expand the number of known *p*-type wide-gap semiconductors, some effort has been directed to the study of oxides containing Rh(III). Rh(III) has a d^6 electron configuration, and in an octahedral environment the 4*d* orbitals split into filled t_{2g}^6 and empty e_g^0 sets. Like the case of the filled d^{10} levels of Cu(I), holes can be introduced into the t_{2g} set to realize *p*-type conductivity. The splitting of the t_{2g} and e_g levels amounts to 2.1 eV in $ZnRh_2O_4$, where a thermally activated conductivity of 0.7 S cm^{-1} and a positive Seebeck coefficient, +0.14 mV K^{-1}, have been reported (Mizoguchi 2001). This composition has also been deposited as an amorphous film onto a-IGZO to yield a *p*-*n* heterojunction diode (Narushima et al. 2003). From TEM imaging, the amorphous rhodium oxide was found to be comprised of 2-3 nm particles. Analysis of the layer spacings in the particles is consistent with the presence of RhO_6 octahedra that provide a percolation pathway for conduction of the holes.

4.4.3 Nanomaterials

While most work in transparent electronics has been focused on the development of compound oxide semiconductors, some effort is being directed to fabrication of devices on the basis of nanostructured solids. We mention here work on carbon nanotube TTFTs (Cao et al. 2006), which have been fabricated on plastic substrates by using transfer printing of single-walled carbon nanotubes. By simply adjusting tube densities, they were used to pattern all of the conducting and semiconducting components of the device. SU8-2 epoxy and the elastomer polydimethylsiloxane (PDMS) were used as dielectrics. The work was largely directed to demonstration of the potential of printing nanostructured solids for realization of flexible devices. Given the very early stages of the technology, it is not surprising that on-to-off ratios (~10^2) and current saturation are quite modest, and mobilities (~30 cm^2 V^{-1} s^{-1}) are extracted at excessively high voltages. Nevertheless, these *p*-type TTFTs are highly transparent (~80%) across the visible and largely unaffected by bending up to a tensile stress of 2%. When the processing of carbon nanotubes with respect to control of conducting and semiconducting properties is optimized, they could play a role in the fabrication of useful TTFTs.

4.4.4 Prospects for *p*-type semiconductors in transparent electronics

The development of robust *p*-type semiconductors for use as channel materials in TTFTs remains a considerable challenge. While significant advances have been made in identifying and depositing new wide band-gap materials for applications in optoelectronics (see Chapter 2), a high-performance *p*-type TTFT has remained elusive. Cu(I) materials would seem to provide a path to the realization of such devices, but thin films exhibiting the desired combination of carrier concentrations, mobilities, and band gaps have yet to be realized. In particular, the inability to deposit a polycrystalline film of LnCuQO or MCuQF with a carrier concentration < 10^{18} cm^{-3} has been a serious impediment to the production of a working device. Improved understanding of defect formation in these systems is required for designing potential experiments to achieve the desired results. Even under optimum conditions, the performance of a *p*-type TTFT with presently available Cu(I) channel materials is likely to considerably lag those fabricated with *n*-type oxide channels. The highest hole mobilities for the epitaxial films of the Cu(I) chalcogenides are more than a factor of 20 lower than the epitaxial films of the *n*-type oxides, and this mobility re-

lationship is likely to persist or worsen in functioning devices, meaning we can expect an upper device mobility of ~1 $cm^2 V^{-1} s^{-1}$ with the current materials set.

From the viewpoint of process integration, *p*-type oxides provide the most desirable materials route to useful devices. Here, the only opportunities have so far been presented by complex Cu(I) and Rh(III) oxides. The hole mobilities of these materials, however, are small, and the band gaps of the Rh(III) compounds are too small to permit transmission across the entire visible portion of the electromagnetic spectrum. Only modest effort has been directed towards an examination of potential wide-gap *p*-type oxides with metals having ns^2 electron configurations. These materials present their own challenges with respect to controlling oxidation states and realizing structural characteristics that will place the *s* level near the top of the valence band, but experiments are worthwhile. As noted above, carbon nanotubes provide an additional route to the realization of a *p*-type TTFT. Like the *p*-type metal oxide and chalcogenide semiconductors, considerable materials development remains, before high-performance devices will be realized.

4.5 Dielectrics

4.5.1 Gate dielectrics

Those actively involved in the pursuit of transparent electronics are already aware of the fact that the development of TTFT gate dielectrics is a more demanding challenge than is that of the channel layer. The quality of the TTFT gate dielectric is an important consideration strongly affecting TTFT performance. An optimal gate dielectric would be amorphous and atomically smooth, while exhibiting a large breakdown field (> ~4 MV/cm), a low leakage current density (< ~10 nA/cm^2 @ 1 MV/cm), a large relative dielectric constant (> ~10), and a low interface state density in conjunction with the channel layer. The availability of such an insulator would greatly affect the performance and stability of TTFTs, as considered in Chapter 5, as well as the required power supply voltage.

Most transparent electronics development involves the use of binary oxide gate insulators, such as SiO_2, Al_2O_3, HfO_2, ZrO_2, or Y_2O_3. Although

binary oxides will undoubtedly be employed for TTFT gate dielectric applications, we contend that the use of a binary oxide is a non-optimal TTFT gate dielectric solution.

There are two primary disadvantages of using a binary oxide. First, binary oxides often have a tendency to crystallize, even at low process temperatures (Wilk et al. 2001; Robertson 2006). An amorphous gate insulator is essential because of the smooth surface requirement (which determines the channel mobility and perhaps the interface state distribution), but also because of deleterious effects associated with grain boundaries, which will detract from TTFT performance, manufacturability, and reliability due to grain boundary related effects such as enhanced impurity interdiffusion and leakage current. Second, an important gate insulator figure-of-merit is the dielectric constant-breakdown field product (Ono 1995). A binary oxide with a high dielectric constant typically has a smaller band gap (the magnitude of which is related to the breakdown field), while a binary oxide with a wide band gap (and hence a larger breakdown voltage) usually has a smaller dielectric constant. Thus, binary insulator optimization involves a trade-off between dielectric constant and breakdown field.

Table 1. Properties of selected binary oxide gate dielectric constituents (Ono 1995; Wilk et al. 2001; Robertson 2006).

Oxide	Dielectric Constant	Bandgap (eV)	Electron affinity (eV)	Crystal Structure
Al_2O_3	9	8.7	0.8	amorphous
Sc_2O_3	~13	~6	?	?
Y_2O_3	15	5.6	1.7	cubic
HfO_2	25	5.7	2.5	monoclinic tetragonal cubic
Ta_2O_5	26	4.5	2.5-3.0	orthorhompic
TiO_2	80	5.3	2.8	tetragonal (rutile, anatase)
ZrO_2	25	5.8	2.6	monoclinic tetragonal cubic

The TTFT gate dielectric solution advocated here is to employ multi-component combinations of the oxides of Al, Sc, Y, Hf, Ta, Ti, and/or Zr. Multi-component combinations are preferred to inhibit crystallization of the gate dielectric, ensuring that it is amorphous. This multi-component

strategy has proven to be highly successful in the development of AOSs used as channel layers in TTFTs. An amorphous gate dielectric will have a smoother surface, thereby improving TTFT channel mobility, manufacturability, and perhaps interface state properties.

The use of a multi-component, rather than a binary oxide offers an improved strategy for maximizing the dielectric constant-breakdown field product, since both high dielectric constant and high breakdown voltage constituents may be incorporated into the gate dielectric. It is possible that this can be successfully accomplished with a compositionally homogeneous multi-component dielectric. However, optimal TTFT gate insulators are likely to be multi-layered or otherwise compositionally inhomogeneous, as discussed in the following.

Of the binary oxides considered in Table 1, Al_2O_3, Y_2O_3, and perhaps Sc_2O_3 are attractive channel-insulator interface constituents since they possess wider band gaps, larger conduction band discontinuities, and negative fixed charge (Wilk et al. 2001). A larger band gap and conduction band discontinuity helps to increase the breakdown voltage and suppress the leakage current. Negative fixed charge aids in obtaining a positive threshold or turn-on voltage for an n-channel device, which is highly desired since it leads to enhancement-mode TTFT operation.

The other binary oxides included in Table 1, HfO_2, Ta_2O_5, TiO_2, and ZrO_2, are more polarizable materials, thus having appreciably larger dielectric constants. Since a high-k gate dielectric is very desirable, there are compelling reasons for incorporating these oxides into the multi-component gate dielectric. However, these materials tend to have a smaller band gap and/or a relatively large electron affinity (a larger electron affinity yields a smaller conduction band discontinuity and, therefore, a smaller carrier injection barrier). A large band gap is desired, especially at the channel-insulator and the insulator-gate interface, to suppress carrier injection into the insulator, which is manifest as a lower breakdown voltage and a higher leakage current density.

Therefore, on the basis of the considerations presented in the previous two paragraphs, multi-layers and compositionally inhomogeneous gates are attractive possibilities, where multi-component combinations of Al_2O_3, Y_2O_3, and perhaps Sc_2O_3 are placed near interfaces to improve the breakdown field and inhibit leakage current, while the central portion of the gate dielectric involves multi-component combinations of HfO_2, Ta_2O_5, TiO_2, and/or ZrO_2 which leads to the realization of a higher-k gate dielectric.

We have recently introduced a unique approach to developing such dielectric materials by extending solution-based spin-on-glass technologies associated with interlevel dielectrics (see Section 4.5.1) in CMOS technology to materials exhibiting higher dielectric constants. A new solution-based platform has been developed for directly addressing and developing the multi-component, multi-layer, and compositionally inhomogeneous features desired in a high-performance, high-k dielectric (Anderson et al. 2007; Meyers et al. 2007).

Numerous compositions, including hafnium and zirconium oxide sulfates and aluminum phosphates, have been deposited directly from organic-free aqueous solutions. The films are atomically dense and exhibit surfaces that are extremely flat (RMS roughness ~0.2 nm). Dielectric characteristics of the sulfates include permittivities covering the range of 9-12, breakdown fields up to 6 MV cm^{-1}, and leakage currents < 10 nA cm^{-2} @ 1 MV cm^{-1}. They have been integrated into TFTs, yielding on-to-off ratios > 10^6 and leakage current densities near 1 nA cm^{-2}. By varying composition in the phosphate system, permittivities in capacitor tests can be controlled across the range 4.8-8.5, and leakage currents are typically < 10 nA cm^{-2} @ 1 MV cm^{-1} with current limited breakdown fields extending to 10 MV cm^{-1}.

The very high quality and smooth surfaces of these films have provided an opportunity to form unique multilayers and the first examples of solution-processed nanolaminates (Anderson et al. 2007). High-order laminates have been formed by stacking as many as 16 individual layers with individual layers as thin as 3 nm, providing a direct means to produce multilayer configurations. Such a capability also provides a number of design tools associated with the interdiffusion of partially hydrated precursors for optimizing the properties of a gate dielectric. The prospects for enhancing device performance are revealed by the use of a 40-nm gate dielectric of aluminum phosphate with an amorphous ZnO-SnO_2 channel layer annealed at 300 ^oC. Here, μ_{inc} = 26 cm^2 V^{-1} s^{-1} at V_{GS} = 10 V and V_{DS} = 1 V with leakage current ~1 nA, values comparable to those achieved with conventional vapor deposition of ZnO-SnO_2 with annealing at 600 ^oC (Hoffmann 2006).

The performance of ZnO-based TFTs has been examined with thin 25-nm dielectrics of HfO_2, $HfSiO_x$, and Al_2O_3 deposited by atomic layer deposition (Carcia 2006). ZnO was deposited via sputtering with no substrate heating. With HfO_2 and $HfSiO_x$ dielectrics, device mobilities are

12.2 and 4.5 $cm^2\ V^{-1}\ s^{-1}$, respectively, in the best case exceeding values observed with a 200-nm thick SiO_2 dielectric by a factor of 30; leakage currents, however, are higher than that of SiO_2 by factors of 10^3-10^4. For those Al_2O_3 films processed above 200 °C, leakage currents are comparable to those of SiO_2. 25-nm thick Al_2O_3 films yield a mobility of 0.5 $cm^2\ V^{-1}\ s^{-1}$, while thicker 100-nm films produce a mobility of 17.6 $cm^2\ V^{-1}\ s^{-1}$.

4.5.2 Interlevel dielectrics

Interlevel dielectrics will be required in transparent electronics integrated circuit applications, where electrical interconnections between devices will sometimes run over or under a channel layer or a TTFT. The function of an interlevel dielectric (Wolf 1990) is to provide electrical isolation between the interconnect and the TTFT. An interlevel dielectric can also act as a passivation layer for the channel layer, electrically protecting it from ambient gases, and as a protection layer from chemical and physical interference during operation. Passivation is discussed further in Section 6.2.2.

A high-k dielectric is advantageous for TTFT gate insulator applications since the objective here is to use a minimal gate voltage to induce carriers into the accumulation layer channel. In contrast, a low-k dielectric is optimal for interlevel dielectric applications since the goal here is to avoid inducing an accumulation layer channel when an electrical signal propagates over or under a channel layer of a TTFT. A wide variety of inorganic and organic dielectrics have been investigated as interlevel dielectrics for deep submicron CMOS applications (Wolf 2002), so that transparent electronics will undoubtedly greatly leverage these developmental efforts. Virtually nothing has appeared in the transparent electronics literature to date regarding the selection or utilization of interlevel dielectrics.

5 Devices

5.1 Transparent electronics devices

In order to produce a transparent-electronics-based system, appropriate materials must be selected, synthesized, processed, and integrated together in order to fabricate a variety of different types of devices. In turn, these devices must be chosen, designed, fabricated, and interconnected in order to construct circuits, each of which has to be designed, simulated, and built in such a way that they appropriately function when combined together with other circuit and ancillary non-circuit subsystems. Thus, this product flow path involves materials → devices → circuits → systems, with each level of the flow more than likely involving multi-feedback iterations of selection, design, simulation, fabrication, integration, characterization, and optimization.

From this perspective, devices constitute a second level of the product flow path. The multiplicity, performance, cost, manufacturability, and reliability of available device types will dictate the commercial product space in which transparent electronics technology will be able to compete. Thus, an assessment of the device toolset available to transparent electronics is of fundamental interest, and is the central theme of this chapter.

Passive, linear devices - resistors, capacitors, and inductors - comprise the first topic discussed. Passive devices are usually not perceived to be as glamorous as active devices, but they can be enabling from a circuit-system perspective, and they are also the simplest device types from an operational point-of-view. Together, these two factors provide the rationale for considering this topic initially.

Next, two-terminal electronic devices - pn junctions, Schottky barriers, heterojunctions, and metal-insulator-semiconductor (MIS) capacitors - constitute the second major topic. The motivation for this topical ordering

is again associated with their relative operational complexity, rather than their utility.

The third and final major topic addressed is transistors. This is the most important matter considered in this chapter. Most of this discussion focuses on TTFTs, since they are perceived to be the most useful type of transistor for transparent electronics. Additionally, a very brief overview of alternative transistor types - static-induction transistors, vertical TFTs, hot electron transistors, and nanowire transistors - is included. This is motivated by recognizing the desirability of achieving higher operating frequencies than are likely obtainable using TTFTs with minimum gate lengths greater than ~2-10 μm, a probable lower-limit dimensional constraint for many types of low-cost, large-area applications. Alternative transistors such as these offer possible routes for reaching higher operating frequencies, in the context of transparent electronics.

5.2 Passive, linear devices

A passive device absorbs energy, in contrast to an active device, which is capable of controlling the flow of energy (Spencer and Ghausi 2003). A linear device is distinguished by the fact that its input-output characteristics are describable using a linear mathematical relationship. The three passive, linear devices of interest are resistors, capacitors, and inductors.

5.2.1 Resistors

An *ideal* resistor is a device whose current-voltage characteristics are linear, described by Ohm's Law, and which dissipates power if a voltage exists across it. The two foundational *ideal* resistor device equations are indicated by the first two entries in Table 5.1.

A *real* resistor may not be perfectly linear, i.e., precisely obey Ohm's Law, and may also possess some undesirable capacitive or inductive parasitic characteristics. Transparent thin-film resistors (TTFRs) are expected to operate at relatively low frequencies, so that parasitic inductance is not anticipated to be relevant. Additionally, TTFRs will most likely be fabricated on insulating substrates, so that parasitic capacitance should be minimal. Finally, if properly designed, a TTFR is expected to exhibit linear or very near-linear behavior. Thus, in most respects, we expect a TTFR to be adequately modeled as an ideal resistor.

Table 5.1. A summary of resistor device equations.

Quantity Assessed	Equation
Voltage (instantaneous)	$v(t) = i(t)R$ (Ohm's Law)
Power dissipated (instantaneous)	$p(t) = i(t)v(t)$
TTFR resistance	$R = \frac{\rho L}{A} = \frac{\rho L}{Wt} = \frac{\rho}{t}\frac{L}{W} = R_S n$

t = time (s)
i(t) = current (instantaneous) (A)
R = resistance (Ω)
ρ = resistivity (Ω-cm)
L = current path length (cm)
A = current path cross-sectional area (A = Wt) (cm^2)
W = current path cross-sectional width (cm)
t = thin-film thickness (cm)
R_S = sheet resistance ($\Omega\ \square^{-1}$)
n = number of squares, i.e. $n = \left.\frac{L}{W}\right|_{L=W}$ (unitless)

An equation for the resistance of a TTFR is given by the third entry in Table 5.1. The resistance depends on a material property, namely the resistivity of the TTFR layer, and the geometry, which is assumed to be rectangular for the situation considered in Table 5.1. Given this geometrical constraint, if the current path length is assumed to be equal to the cross-sectional width, i.e., if L = W, and if a sheet resistance is defined as $R_S = \rho/t$, then the resistance depends simply on R_S and the number of resistor squares in the TTFR layout.

Figure 5.1a shows a plan-view of a straight-line or linear TTFR. The TTFR path consists of 16 squares, with two larger end squares, generically illustrating one possible resistor termination scheme. Many variations on resistor termination are possible. A more complicated, meandering TTFR layout with 36 path squares is given in Figure 5.1b. This TTFR occupies approximately the same area as the straight-line TTFR of Fig. 5.1a, but possesses a larger resistance because of the larger number of squares in its path and also due to the existence of bends in the meander structure, which increase the resistance (Glaser and Subak-Sharpe 1979; Elshabini-Riad and Barlow 1998).

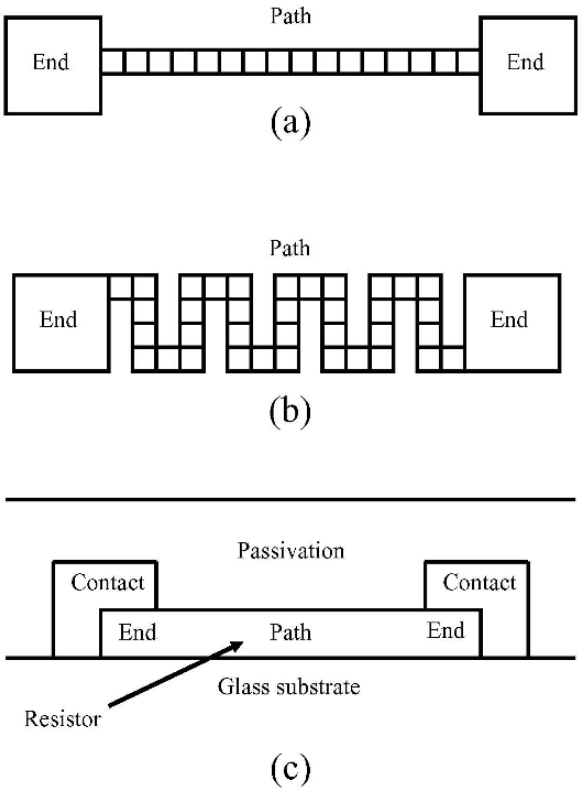

Fig. 5.1. (a) Plan-view of a straight-line or linear transparent thin-film resistor (TTFR) and (b) a meander TTFR. (c) Cross-sectional view of a TTFR in which contacts and passivation are also indicated.

Figure 5.1c offers a cross-sectional view of a TTFR in which the resistor path and ends have the same thickness, which need not always be the case. Contacts from the resistor ends to other locations on the substrate are indicated, as is a passivation layer. If the TTFR layer is heavily doped, e.g., ITO, the passivation layer's role is merely to provide physical and chemical protection. However, it is possible that a passivation layer may actually play an active role in establishing the TTFR resistance if a highly insulating layer is used in the resistor path and its conductance is established by creation of a surface accumulation layer due to the presence of the passivation layer. In this case, the resistance would not scale with the TTFR thickness, but would be controlled by the surface accumulation charge due to interface properties and charge within the passivation layer.

TTFR sheet resistances of ~10-10^5 Ω/□ should be possible, using doped TCOs such as ITO or undoped TTFT channel layers such as ZTO. Thus, a wide range of TTFR resistance is possible.

Two thin-film resistor concerns are the desire to have a small temperature coefficient of resistance (TCR) and resistor tolerance. Near-zero temperature coefficient of resistance values have been demonstrated for antimony-doped SnO_2, with an appropriate doping concentration (Maissel and Glang 1970). TTFR resistance tolerance is expected to be similar to that of conventional thin-film resistors, ±10%, unless resistor trimming is performed, in which case a tolerance of approximately ±0.1% is possible (Glaser and Subak-Sharpe 1979; Elshabini-Riad and Barlow 1998). It is not clear whether resistor trimming will be practical in a transparent electronics technology, given its anticipated low-cost structure. Smooth surfaces are highly desirable for TTFR applications, suggesting that amorphous layers would be preferred.

5.2.2 Capacitors

An *ideal* capacitor is an electric field energy storage device possessing linear current-voltage derivative (i-dv/dt) characteristics. Defining ideal capacitor equations are collected in the first three entries of Table 5.2.

Table 5.2. A summary of capacitor device equations.

Quantity Assessed	Equation
Charge (instantaneous)	$q(t) = Cv(t)$
Current (instantaneous)	$i(t) = C\dfrac{dv(t)}{dt}$
Energy stored (instantaneous)	$w(t) = \dfrac{1}{2}C[v(t)]^2$
TTFC capacitance	$C = \dfrac{\varepsilon_I A}{d_I} = \dfrac{\varepsilon_I LW}{d_I}$
t = time (s) C = capacitance (F) v(t) = voltage (instantaneous) (V) ε_I = insulator dielectric constant (F cm^{-1}) A = capacitor area (A = LW; see Fig. 5.2) (cm^2) d_I = dielectric thickness (cm)	

A plan-view and a cross-sectional view of a transparent thin-film capacitor (TTFC) are given in Fig. 5.2. In order for this device to be completely transparent, all of the layers should be transparent. Most insulators are transparent, so that this constraint mainly applies to the contact layers, which will most likely be highly conducting TCOs such as ITO. Alternative TTFC structures, e.g., interdigitated capacitors (Glaser and Subak-Sharpe 1979; Elshabini-Riad and Barlow 1998), are possible in addition to the simple TTFC structure shown in Fig. 5.2.

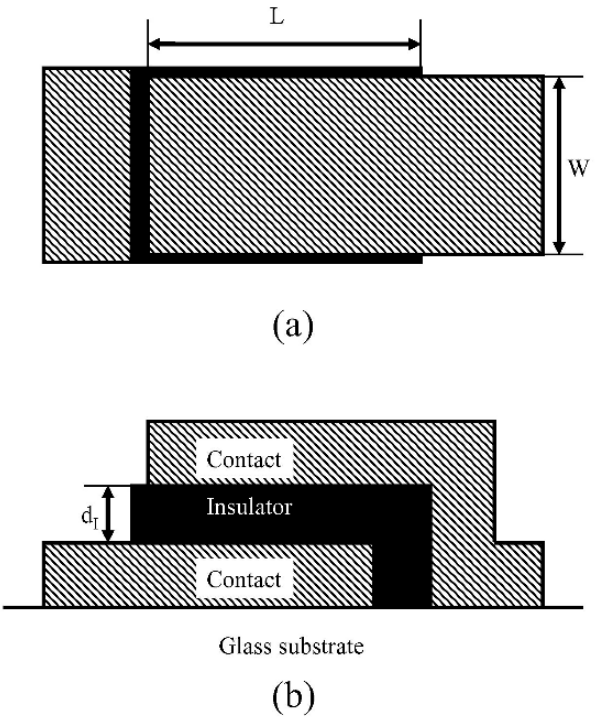

Fig. 5.2. (a) Plan-view and (b) cross-sectional view of a transparent thin-film capacitor (TTFC).

The primary TTFC design equation is included as the fourth entry in Table 5.2. The TTFC capacitance is established by the capacitance density, i.e., the capacitance per unit area, of the basic capacitance stack, i.e., ε_S/d_I, and the geometric area of the capacitor layout. Usually a large capacitance density is desired, in order to minimize the size of a capacitor. Therefore, a thin insulator with a high dielectric constant (sometimes re-

ferred to as a 'high-k dielectric', where 'k' denotes the relative dielectric constant) is best. However, a high-k dielectric typically has a smaller bandgap, which usually results in a low breakdown electric field. Although reducing the insulator thickness also increases the capacitance density, a minimum thickness is required to avoid pinholes and other types of defects which degrade the breakdown field and which yield more insulator leakage. Optimal TTFC and TTFT gate insulators will have maximal dielectric constant-breakdown field products (Ono 1995). For a more detailed discussion of insulators and thin-film capacitors the interested reader is referred to the following references (Maissel and Glang 1970; Glaser and Subak-Sharpe 1979; Elshabini-Riad and Barlow 1998; Ono 1995; Kao 2004).

Real TTFCs are expected, for most purposes, to be accurately modeled as *ideal* capacitors. Although TTFC performance may be degraded by inductive and resistive parasitic effects, neither of these are expected to be severe given that these devices are expected to be used at relatively low frequencies and that low-leakage thin-film insulators are already employed in non-transparent applications. From process integration, manufacturability, and reliability considerations, TTFC contacts and insulators should ideally be amorphous.

5.2.3 Inductors

An *ideal* inductor is a magnetic field energy storage device possessing linear voltage-current derivative (v-di/dt) characteristics. Important ideal inductor equations are collected in the first two entries of Table 5.3.

In contrast to a TTFR and a TTFC, a transparent thin-film inductor (TTFI) and related transparent magnetically-coupled devices are expected to behave in a non-ideal manner. Two main reasons underlie this expectation. First, because of the relatively poor conductance of TCOs compared to metals, TTFIs will possess a significant amount of parasitic resistance. Second, efficient magnetic field coupling is strongly facilitated by the use of a magnetically-permeable insulator. However, we are not aware of a transparent, magnetically-permeable insulator material. Thus, realizing high performance TTFIs and related magnetically-coupled devices is expected to be a challenging task.

The last two entries included in Table 5.3 are useful for understanding certain aspects of TTFI non-idealities. The quality factor, Q, is basically an inductor performance figure-of-merit. A larger Q is better. Thus, since the parasitic resistance of a TTFI is expected to be large, as a consequence

of employing a TCO instead of a metal, high-Q TTFI's are not expected. The last entry in Table 5.3 indicates that obtaining a large inductance, L, requires the inductor to cover a large area and to possess a large number of turns. The large-area requirement is not necessarily problematic, since 'real estate' if often 'free' in transparent electronics. However, needing to have a large number of turns is likely to cause trouble, since having a large number of turns will increase the inductor parasitic series resistance, and probably also the inductor parasitic capacitance.

Table 5.3. A summary of inductor device equations.

Quantity Assessed	**Equation**
Voltage (instantaneous)	$v(t) = L\dfrac{di(t)}{dt}$
Energy stored (instantaneous)	$w(t) = \dfrac{1}{2}L[i(t)]^2$
Quality factor	$Q = \dfrac{2\pi fL}{R_L}$
Inductance (rectangular spiral inductor)	$L \propto SN^2$ (Kovacs 1998)
t = time (s) L = inductance (H) i(t) = current (instantaneous) (A) f = frequency (Hz) R_L = inductor parasitic resistance (Ω) S = maximum side dimension (cm) N = number of turns (unitless)	

These TTFI challenges are disappointing since a TTFI and its magnetically-coupled device variants are potentially application-enabling, performance-enhancing components. Inductors are useful in resonant circuits and filters. They can also function as power supply chokes (limiting current fluctuations), energy storage devices for switched-mode power supplies, etc. Furthermore, magnetically-coupled inductors may be used for the construction of transformers for power and signal conditioning. Finally, a somewhat-related application is that of an antenna to transmit or receive rf signals. In this regard, we note that a transparent microwave antenna constructed using ITO has been reported (Outaleb et al. 2000).

Even though a TTFI with good performance appears to be difficult to construct, the benefits of magnetic field coupling devices appear to offer enough enticements to warrant further investigation.

5.3 Two-terminal devices

There are four types of two-terminal semiconductor devices: pn junctions, Schottky barriers, heterojunctions, and metal-insulator-semiconductor (MIS) capacitors. These devices are fundamental, since all more complicated three-terminal and multi-terminal semiconductor electronic devices consist of combinations of these basic two-terminal devices. Thus, each two-terminal device is briefly and individually considered in the following four subsections, within the framework of transparent electronics.

5.3.1 pn junctions

A strong argument can be made that the pn junction is the most fundamental semiconductor device, in terms of semiconductor device explication and functionality. Therefore, our contention that a pn junction is a relatively unimportant transparent electronics device, at least for present and near-future state-of-the-art, may seem somewhat heretical. Our rationale for this assertion is that we believe that early-stage transparent electronics will be primarily a *unipolar* rather than a *bipolar* technology. Let's explore this assertion in more detail.

Bipolar device operation depends on the availability of both carrier types - electrons and holes - and is, to a large extent, dominated by **minority carrier action** (Pierret 1996; Taur and Ning 1998; Sze and Ng 2007). Although a pn junction is the simplest possible bipolar device, it has a wide range of applications, including its use as a rectifier, varistor, varactor, temperature sensor, solar cell, photodiode, light-emitting diode (LED), and laser. A pn junction is also a critical constituent of many types of more complicated bipolar devices, including a bipolar junction transistor, a thyristor, an insulated-gate bipolar transistor, and a MOS-gated thyristor.

In contrast to a bipolar device, the operation of a *unipolar* device depends, to a large extent, on only **one carrier type**. Examples of unipolar devices include Schottky barriers, TFTs, TTFTs, and field-effect transistors (FETs).

There are two main reasons why unipolar devices are better suited to transparent electronics applications. First, visible transparency mandates the use of wide band gap semiconductors. It is difficult, and often impossible, to obtain bipolar doping in many of these materials, which have a strong tendency to remain either strongly insulating or unipolar, probably as a consequence of their tendency towards vacancy self-compensation (Kröger 1974; Van Vechten 1980; Wager 1993; Wager et al. 2002). Second, efficient bipolar operation requires long **minority carrier lifetimes**. In turn, this minority carrier lifetime requirement usually mandates the use of single crystals (Teal 1976). We think that the use of single crystal materials will be cost-prohibitive in most transparent electronics applications, in which polycrystalline or amorphous materials will predominate.

There are many transparent electronics applications which would greatly benefit from the availability of a pn junction. In particular, a low-cost, large-area inorganic-LED (ILED) would be immensely useful for transparent displays and for other important and elusive applications. Although we do not expect to see ILEDs or other transparent bipolar device types commercially available in the near future, given their obvious utility, it is possible that they may emerge sooner than we expect. To encourage this type of development, we offer the following thoughts regarding their realization.

First, we believe that anisotype (i.e., pn) heterojunctions offer a better route to the realization of an ILED than a conventional pn homojunction, given the tendency for a wide band gap semiconductor to undergo self-compensation. Second, if layers approaching single crystal quality can be grown at low-cost and over large areas, this is probably the best way to proceed since these materials will have better performance than poorer crystallinity devices. This will require perfecting novel growth strategies similar to those under development for silicon-based applications, such as metal-induced crystallization or continuous-grain silicon growth (Kuo 2004b). Fourth, polycrystalline bipolar devices may also be feasible if minority carrier reflecting grain boundaries, such as those observed in Cu-$InSe_2$ solar cells, can be designed using wider band gap transparent materials (Persson and Zunger 2003; Hetzer et al. 2005). Fifth, bipolar amorphous semiconductors would be ideal for transparent electronics, in terms of cost and manufacturability, if their minority carrier lifetime properties were good enough; this appears to be a difficult challenge.

Since we have argued that a pn junction is not, at this time, an important transparent electronics device, it is best to now terminate any further dis-

cussion of this device, except for the inclusion of Table 4.4 which provides a concise summary of significant pn junction device physics equations. A list of relevant device physics equations will be given for most of the other devices considered in the remainder of this chapter.

Table 5.4. A summary of pn junction device equations.

Quantity Assessed	Equation
Built-in potential	$V_{BI} = \frac{k_B T}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$
Depletion width	$W = \sqrt{\frac{2\varepsilon_S (N_A + N_D)(V_{BI} - V)}{q N_A N_D}}$
Diffusivity	$D_{n,p} = \frac{k_B T}{q} \mu_{n,p}$
Diffusion length	$L_{n,p} = \sqrt{D_{n,p} \tau_{n,p}}$
Current density (diffusion)	$J = q n_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)\left[\exp\left(\frac{qV}{k_B T}\right) - 1\right]$
Generation-recombination lifetime	$\tau = \frac{1}{\sigma v_{th} N_t}$
Current density (generation-recombination)	$J = \frac{q n_i W}{2\tau}\left[\exp\left(\frac{qV}{2k_B T}\right) - 1\right]$

k_B = Boltzmann's constant (J K^{-1})
T = temperature (K)
q = electronic charge (C)
$N_{A,D}$ = acceptor, donor doping density (cm^{-3})
n_i = intrinsic carrier concentration (cm^{-3})
ε_S = semiconductor dielectric constant (F/cm^2)
V = applied voltage (forward bias = +, reverse bias = -) (V)
$\mu_{n,p}$ = electron, hole mobility ($cm^{-2}V^{-1}s^{-1}$)
σ = midgap trap capture cross-section (cm^2)
v_{th} = thermal velocity (cm s^{-1})
N_t = midgap trap density (cm^{-3})

5.3.2 Schottky barriers

To appreciate Schottky barriers at a fundamental level, our first task is to elucidate Schottky barrier formation from an energy band diagram perspective (Wager 2007).

To do this, begin with a metal-semiconductor junction according to **ideal** Schottky barrier theory, as illustrated by the energy band diagrams shown in Fig. 5.3. Figure 5.3a depicts an energy band diagram for an isolated metal and an isolated n-type semiconductor (valence band not shown) in terms of the metal and semiconductor work functions, Φ_M & Φ_S, and the semiconductor electron affinity, χ_S. When the metal and semiconductor of Fig. 5.3a are brought into intimate contact, electron transfer occurs from the semiconductor to the metal, giving rise to the formation of a *macroscopic* negative *dipole*, as indicated by the lower left-pointing arrow in Fig. 5.3a. This *dipole* consists of a negative interfacial charge sheet which is balanced by an equal density of positive charge in an extended space charge region within the semiconductor. Such a dipole is denoted *macroscopic* since the sheet of negative interfacial charge and the charge-centroid of the space charge region charge define a dipole with a spatial dimension on the order of the space charge region dimension. The direction of charge transfer, and hence the polarity of the dipole, is determined by the relative Fermi level positions of the metal and semiconductor.

Figure 5.3b shows an energy band diagram for the Schottky barrier formed after the metal and semiconductor come into intimate contact for this ideal model case. The effect of charge transfer is evident from the positive curvature of the semiconductor conduction band near the interface. Two electronic barriers are established as a consequence of this interfacial charge transfer; the n-type semiconductor Schottky barrier height, φ_{Bn}, and the built-in potential, V_{BI}. Each of these barriers acts to inhibit electron transfer in opposing directions across the interface. The presence of a majority carrier barrier in the semiconductor means that this metal-semiconductor junction will function as a Schottky barrier, which in turn means that it will be characterized by rectifying, i.e., diode-like, current-voltage curves. An important feature of this ideal model interface is the fact that the local vacuum level is continuous across the interface.

In summary, **ideal** Schottky barrier formation is a consequence of Fermi-level-mediated charge transfer, giving rise to a *macroscopic* interfacial *dipole*.

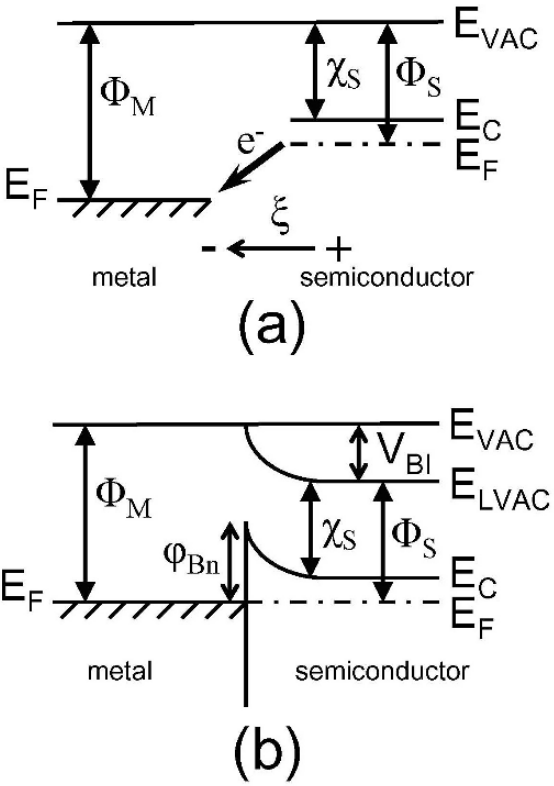

Fig. 5.3. Energy band diagrams for (a) an isolated metal and an isolated n-type semiconductor (valence band not shown) with $\Phi_M > \Phi_S$, and (b) the corresponding Schottky barrier band structure for an ideal interface (i.e., charge exchange is exclusively Fermi-level mediated, as indicated by the upper arrow shown in (a)). Ideal charge exchange results in the formation of a *macroscopic* negative *dipole*, as indicated by the bottom arrow in (a). This figure was published in Thin Solid Films, J F Wager, Transparent electronics: Schottky barrier and heterojunction considerations, Copyright Elsevier (2007).

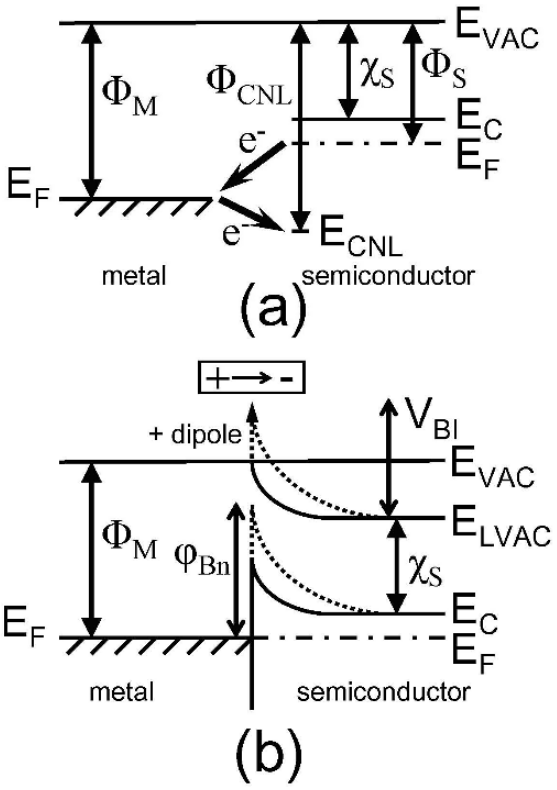

Fig. 5.4. Energy band diagrams for (a) an isolated metal and an isolated n-type semiconductor (valence band not shown) with $\Phi_M > \Phi_S$ and with $\Phi_M < \Phi_{CNL}$, and (b) the corresponding Schottky barrier band structure for a non-ideal interface (i.e., charge exchange is Fermi-level-mediated, as indicated by the upper arrow shown in (a) and also occurs by misalignment of the metal Fermi-level and the semiconductor charge neutrality level (lower arrow in (a)). Non-ideal charge exchange results in the formation of a *microscopic* positive dipole, as indicated in (b). This figure was published in Thin Solid Films, J F Wager, Transparent electronics: Schottky barrier and heterojunction considerations, Copyright Elsevier (2007).

Next, consider the formation of a metal-semiconductor junction from the perspective of **non-ideal** Schottky barrier theory, as indicated in Fig. 5.4. This non-ideal situation is identical to the ideal case shown in Fig. 5.3 except for the inclusion of a charge neutrality level, E_{CNL}, at the semiconductor surface. Physically, a charge neutrality level corresponds to the branch point within the semiconductor band gap, above (below) which an interface state is predominantly conduction (valence) band derived, or ac-

ceptor-like (donor-like) (Robertson 2000; Monch 2001). From an interface formation perspective, E_{CNL} is an energy established by the nature of the bulk semiconductor band structure, and whose relative alignment establishes the direction of non-ideal charge transfer during interface formation. Thus, in addition to the ideal Fermi-level-mediated charge transfer discussed with respect to Fig. 5.3, a second, non-ideal charge transfer occurs due to misalignment of the metal Fermi-level and the semiconductor charge neutrality level, as indicated by the bottom, right-going arrow shown in Fig. 5.4a. This non-ideal charge exchange results in the formation of a positive *microscopic dipole*, of atomic dimensions, as indicated in Fig. 5.4b, and a concomitant increase in ϕ_{Bn}, and V_{BI}, compared to their corresponding ideal model values (solid lines). Note that the interfacial dipole makes the local vacuum level discontinuous at the interface according to this non-ideal model.

In summary, **non-ideal** Schottky barrier formation is a consequence of charge-neutrality-level-mediated charge transfer, giving rise to a *microscopic* interfacial *dipole*.

The **non-ideal** model situation complementary to that shown in Fig. 5.4 (in which $\Phi_M > \Phi_S$), is given in Fig. 5.5 (in which $\Phi_M < \Phi_S$). Ideal Fermi-level-mediated charge transfer occurs in opposite directions in Figs. 5.4 and 5.5, while non-ideal charge-neutrality-mediated charge transfer occurs in the same direction. If ideal charge transfer dominates for the case shown in Fig. 5.5, this leads to the formation of a negative Schottky barrier height, i.e., majority carriers in the semiconductor do not see an interfacial energy barrier, thereby establishing this contact as Ohmic. An Ohmic contact means that current flow occurs readily, independent of which voltage polarity is applied to the metal, since there is no appreciable barrier to the flow of charge across the metal-semiconductor interface. An Ohmic contact is ideally characterized by a linear (non-rectifying) current-voltage curve with a large slope (indicative of a small resistance).

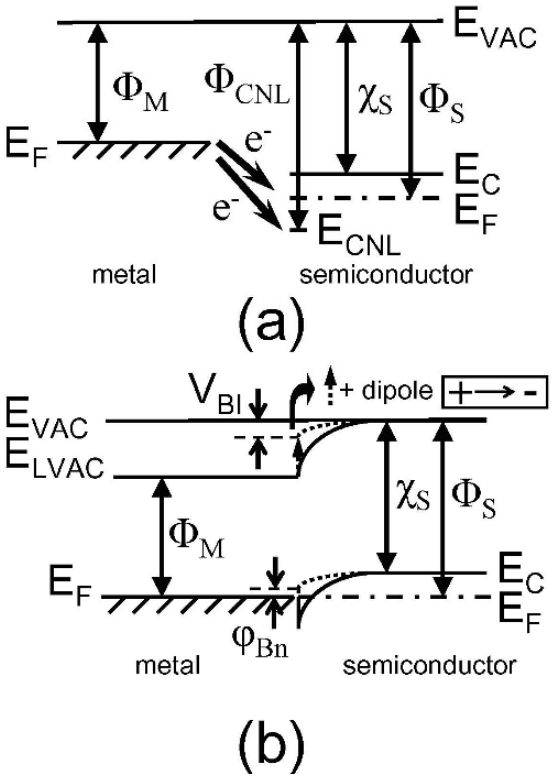

Fig. 5.5. Energy band diagrams for (a) an isolated metal and an isolated n-type semiconductor (valence band not shown) with $\Phi_M < \Phi_S$ and $\Phi_M < \Phi_{CNL}$, and (b) the corresponding Schottky barrier band structure for a non-ideal interface (i.e., charge exchange is Fermi-level-mediated, as indicated by the upper arrow shown in (a) and also occurs by misalignment of the metal Fermi-level and the semiconductor charge neutrality level (lower arrow in (a)). Non-ideal charge exchange results in the formation of a *microscopic* positive dipole, as indicated in (b). This figure was published in Thin Solid Films, J F Wager, Transparent electronics: Schottky barrier and heterojunction considerations, Copyright Elsevier (2007).

Table 5.5. A summary of Schottky barrier interface formation equations. This table is based off of a table published in Thin Solid Films, J F Wager, Transparent electronics: Schottky barrier and heterojunction considerations, Copyright Elsevier (2007).

Quantity Assessed	Equation
Schottky barrier height (n-type)	$\phi_{Bn} = \Phi_M - \chi_S + \Delta_{SB}$
Built-in potential (n-type)	$V_{BI}^{nSB} = \Phi_M - \Phi_S + \Delta_{SB}$
Schottky barrier height (p-type)	$\phi_{Bp} = IP_S - \Phi_M - \Delta_{SB}$
Built-in potential (p-type)	$V_{BI}^{pSB} = \Phi_S - \Phi_M - \Delta_{SB}$
Microscopic dipole correction	$\Delta_{SB} = (1-S)(\Phi_{CNL} - \Phi_M)$
Interface parameter	$S = \dfrac{1}{1 + 0.1(\varepsilon_\infty - 1)^2}$

Φ_M = metal work function (V)
χ_S = semiconductor electron affinity (V)
Φ_S = semiconductor work function (V)
IP_S = semiconductor ionization potential ($IP_S = \chi_S + E_G$) (V)
Φ_{CNL} = semiconductor charge neutrality level (V)
ε_∞ = semiconductor high-frequency relative dielectric constant (unitless)

A quantitative formulation of **non-ideal** Schottky barrier theory is summarized in Table 5.5. Several comments regarding this formulation are warranted. First, the ideal Schottky barrier model obtains if the microscopic dipole correction term, Δ_{SB}, is equal to zero. Thus, this non-ideal model formulation includes the ideal model as a limit when one non-ideal model parameter, Δ_{SB}, goes to zero. Second, assessment of the equation for Δ_{SB} reveals that non-ideal charge transfer depends upon misalignment of the semiconductor charge neutrality level and the metal Fermi level, i.e., (Φ_{CNL}-Φ_M), and also upon (1-S), which physically is related to the electronic screening properties of the semiconductor, as reflected by the magnitude of its high-frequency relative dielectric constant, ε_∞. In the no screening limit, the ideal model again obtains, i.e., $\varepsilon_\infty \rightarrow 1$, so that $S \rightarrow 1$ and $\Delta_{SB} \rightarrow 0$. In the perfect screening limit, the Fermi-level pinning condition (i.e., interfacial energy barriers are metal-independent) results, i.e., $\varepsilon_\infty \rightarrow \infty$, so that $S \rightarrow 0$, $\Delta_{SB} \rightarrow (\Phi_{CNL}\text{-}\Phi_M)$, $\phi_{Bn} \rightarrow (\Phi_{CNL}\text{-}\chi_S)$, and $V_{BI}^{nSB} \rightarrow (\Phi_{CNL}\text{-}\Phi_S)$. (1-S) represents the fraction of the metal Fermi level - semiconductor charge neutrality level misalignment that contributes to the microscopic interfacial dipole after semiconductor screening is taken into account. Third, the sign and magnitude of Δ_{SB} directly establish the sign and magnitude of

the local vacuum level discontinuity, and also modifies the barriers ϕ_{Bn} and V_{BI}^{nSB} compared to their ideal model values, as illustrated by the energy band diagrams shown in Figs. 5.4 and 5.5.

Table 5.6. A summary of Schottky barrier device equations.

Quantity Assessed	Equation
Depletion width	$W = \sqrt{\frac{2\varepsilon_S (V_{BI} - V)}{qN}}$
Current density	$J = A^* T^2 \exp\left(\frac{-q\phi_B}{k_B T}\right)\left[\exp\left(\frac{qV}{nk_B T}\right) - 1\right]$

ε_S = semiconductor dielectric constant (F cm^{-1})
V_{BI} = built-in potential (V)
V = applied voltage (forward bias = +, reverse bias = -) (V)
q = electronic charge (C)
N = doping density (cm^{-3})
A^* = effective Richardson constant (Sze and Ng 2007) (unitless)
T = temperature (K)
ϕ_B = Schottky barrier height (V)
k_B = Boltzmann's constant J K^{-1})
n = ideality factor (Ng 2003; Sze and Ng 2007) (unitless)

In summary, Schottky barrier trends are qualitatively and quantitatively treated in terms of **ideal** (Fermi-level-mediated) and **non-ideal** (charge-neutrality-level-mediated) charge transfer, giving rise to *macroscopic* and *microscopic dipoles* for the ideal and non-ideal model cases, respectively.

This completes our general discussion of Schottky barrier interface formation theory. What is its relevance to transparent electronics? There are two main application venues of Schottky barrier interface formation theory to transparent electronics.

First, a quantitative assessment of Schottky barrier device equations, as summarized in Table 5.6, requires numerical estimates of the Schottky barrier height, ϕ_B, and the built-in potential, V_{BI}. Schottky barrier theory provides a means for estimating these quantities. Note that only ϕ_B is included in Table 5.7 since it is independent of the channel doping density while V_{BI} depends on the doping density of the channel.

Table 5.7. A summary of Schottky barrier interface formation assessment for several types of TTFT ITO-channel layer source-drain contacts (Wager 2007). Non-ideal Schottky barrier theory is used to estimate ϕ_{Bn}; ideal Schottky barrier theory estimates for ϕ_{Bn} are obtained by subtracting Δ_{SB} from those given in the last column of this table. For this assessment, it is assumed that Φ_M(ITO)=4.1 V.

Channel	χ_S (V)	ε_∞ (unitless)	Φ_{CNL} (V)	Δ_{SB} (V)	ϕ_{Bn} (V)
ZnO	4.57	3.85	4.9	+0.36	-0.11
SnO_2	4.5	3.9	5.15	+0.48	+0.08
In_2O_3	4.45	3.7	5.35	+0.53	+0.18

Second, Schottky barrier theory provides some a framework for understanding the physics of transparent electronics electrical contacts and is employed in Section 5.3.4.2 in a discussion of Ohmic contacts to p-channel TTFTs. Note that source and drain TTFT contacts and other types of electrical contacts in a globally transparent application require the use of unconventional 'metals'. To date, the most commonly used transparent electronics 'metal' is ITO, a strongly degenerately doped wide band gap semiconductor. When we employ ITO as a TTFT source (drain) contact, we want it to function as an 'Ohmic' contact, supplying (removing) carriers from the channel as required by the polarity and magnitude of the relevant applied voltage. However, this type of an electrical contact is not typical of a semiconductor contact since a 'normal' metal is not used and the channel layer to which contact is made is highly insulating, rather than moderately to strongly conducting. Therefore, in recognition of these anomalous characteristics, we prefer to refer to well-functioning TTFT source and drain contacts as 'injecting' and 'extracting', respectively.

If we assess an ITO-channel layer contact using non-ideal Schottky barrier interface formation theory, we obtain the results summarized in Table 4.7. For all three of the channel layers considered, the Schottky barrier height is estimated to be either negative, as expected for an Ohmic contact, or positive but with a very small magnitude (these estimates are subject to various uncertainties, as discussed in (Wager 2007)). Once it is recognized that the separation energy between the semiconductor bulk conduction band minimum and the Fermi level is $\geq \sim 0.15$ eV (since the semiconductor is highly insulating, with a carrier concentration less than $\sim 10^{16}$ cm^{-3}), it is clear that channel electrons will see a negative or a negligibly small barrier from the perspective of thermionic emission over the barrier. Thus, the ϕ_{Bn}'s given in Table 5.7 are consistent with injecting contact behavior, as

is empirically known to be the actual situation for these three channel materials (Hoffman et al. 2003; Presley et al. 2004; Chiang et al. 2007).

5.3.3 Heterojunctions

Since our heterojunction interface formation explication is strongly analogous to that presented in Section 5.2.2 for the Schottky barrier, our treatment may be shortened (Wager 2007).

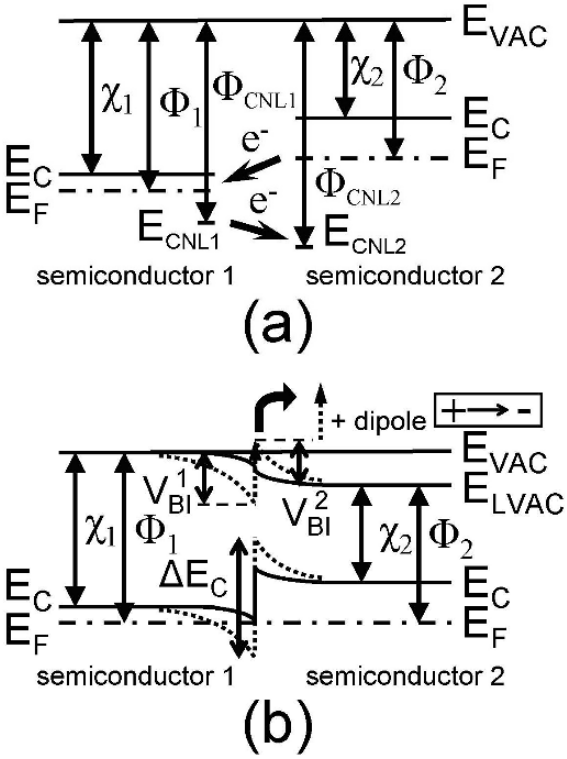

Fig. 5.6. Energy band diagrams for (a) two isolated n-type semiconductors (valence bands not shown) with $\Phi_2 < \Phi_1$, $\chi_2 < \chi_1$, and $\Phi_{CNL2} > \Phi_{CNL1}$, and (b) the corresponding heterojunction band structure for a non-ideal interface (i.e., charge exchange is Fermi-level-mediated, as indicated by the arrow upper shown in (a) and also occurs by misalignment of the semiconductor charge neutrality levels (lower arrow in (a)). Non-ideal charge exchange results in the formation of a *microscopic* positive dipole, as indicated in (b). This figure was published in Thin Solid Films, J F Wager, Transparent electronics: Schottky barrier and heterojunction considerations, Copyright Elsevier (2007).

Figure 5.6 presents an example of the formation of an nn isotype heterojunction from the perspective of **non-ideal** heterojunction theory. Figure 5.6 is the heterojunction analog of the Schottky barrier case shown in Fig. 5.4. Two types of charge transfer are relevant: ideal Fermi-level-mediated charge transfer giving rise to the formation of macroscopic dipole and charge-neutrality-level-mediated charge transfer giving rise to the formation of a microscopic dipole. In this respect, the mechanisms responsible for Schottky barrier and heterojunction formation are identical. As evident from a close comparison of Figs. 5.4 and 5.6, the essential heterojunction differences are that the built-in potential is partitioned across both semiconductors, and the conduction band discontinuity, ΔE_C, plays an analogous role to that of the Schottky barrier height, ϕ_B.

Table 5.8. A summary of heterojunction interface formation equations. This table is based off of a table published in Thin Solid Films, J F Wager, Transparent electronics: Schottky barrier and heterojunction considerations, Copyright Elsevier (2007).

Quantity Assessed	Equation
Conduction band discontinuity	$\frac{\Delta E_C}{q} = \chi_1 - \chi_2 + \Delta_{HJ}$
Built-in potential (n-type)	$V_{BI}^{nHJ} = \Phi_1 - \Phi_2 + \Delta_{HJ}$
Valence band discontinuity	$\frac{\Delta E_V}{q} = IP_2 - IP_1 - \Delta_{HJ}$
Built-in potential (p-type)	$V_{BI}^{pHJ} = \Phi_2 - \Phi_1 - \Delta_{HJ}$
Microscopic dipole correction	$\Delta_{HJ} = (1 - S_{12})(\Phi_{CNL2} - \Phi_{CNL1})$
Interface parameter	$S_{12} = \frac{1}{1 + 0.1\frac{(\varepsilon_{\infty 1} - 1)^2 (\varepsilon_{\infty 2} - 1)^2}{(\varepsilon_{\infty 1} - 1)^2 + (\varepsilon_{\infty 2} - 1)^2}}$

q = electronic charge (C)
$\chi_{1,2}$ = semiconductor electron affinities (V)
$\Phi_{1,2}$ = semiconductor work functions (V)
$IP_{1,2}$ = semiconductor ionization potentials ($IP = \chi + E_G$) (V)
$\Phi_{CNL1,2}$ = semiconductor charge neutrality levels (V)
$\varepsilon_{\infty 1,2}$ = semiconductor high frequency relative dielectric constants (unitless)

Table 5.8 is a summary of heterojunction interface formation equations. Note that this table strongly resembles Table 5.5 in which Schottky barrier interface formation equations are summarized. This similarity is not sur-

prising once it is recognized that a heterojunction becomes a Schottky barrier in the limit of high carrier concentration in semiconductor 1, such that this degenerate semiconductor can be considered to be a metal; i.e., in the strongly degenerate semiconductor doping limit, $\varepsilon_{\infty 1} \rightarrow \infty$, so that $S_{12} \rightarrow S_2$; additionally, $\Phi_{CNL1} \rightarrow \Phi_M$, and $\Delta E_C \rightarrow \phi_{Bn}$; making notational changes in order to be consistent with Schottky barrier nomenclature: $S_2 \rightarrow S$, $\Phi_{CNL2} \rightarrow \Phi_{CNL}$, and $\chi_2 \rightarrow \chi_S$; this results in first two equations of Table 5.8 being equal to the first two equations in Table 5.5.

Instead of assessing these ITO-channel layer contacts using non-ideal Schottky barrier theory (as presented in Table 5.7), it is possible to use non-ideal heterojunction theory to model this type of interface formation. The results of such an analysis are summarized in Table 5.9. Note that both ITO-ZnO and ITO-SnO_2 contacts are expected to behave as injecting contacts, since the conduction band discontinuity, $\Delta E_C/q$, is negative. This is consistent with what is found empirically in TTFTs (Hoffman et al. 2003; Presley et al. 2004). The ITO-In_2O_3 barrier is calculated to be zero using non-ideal heterojunction theory since both of these materials are modeled as In_2O_3. In this case, injecting contact behavior would be expected since this situation actually corresponds to that of a heavily-doped, n^+-n homojunction (Smith 1978).

Table 5.9. A summary of heterojunction assessment for several types of TTFT ITO-channel layer source-drain contacts (Wager 2007). Non-ideal heterojunction theory is used to estimate $\Delta E_C/q$; ideal heterojunction theory estimates for $\Delta E_C/q$ are obtained by subtracting Δ_{HJ} from those given in the last column of this table. For this assessment, it is assumed that χ_S(ITO)=4.45 V.

Channel	χ_S (V)	ε_∞ (unitless)	Φ_{CNL} (V)	Δ_{HJ} (V)	$\Delta E_C/q$ (V)
ZnO	4.57	3.85	4.9	-0.13	-0.25
SnO_2	4.5	3.9	5.15	-0.06	-0.11
In_2O_3	4.45	3.7	5.35	0	0

A summary table of device equations is not included for heterojunctions since different sets of equations exist for pn anisotype and nn or pp isotype heterojunctions. Moreover, these equations appear to be of limited utility to present-day transparent electronics purposes since we believe that the performance of most heterojunctions will be dominated by interface and bulk trapping, such that the idealized equations available in the literature are unlikely to be quantitatively useful. It is recommended that the interested reader consult the literature for a review of heterojunction device equations (Wolfe et al. 1989; Ng 2003; Sze and Ng 2007).

Certain aspects of heterojunction formation theory are employed in Section 6.2.2 with respect to the passivation of TTFT channel layers.

5.3.4 Metal-insulator-semiconductor (MIS) capacitors

Figure 5.7 shows energy band diagrams of flat-band, accumulation, and depletion for an n-type semiconductor in which the doping is ~10^{13}-10^{16} cm^{-3}, which is typical for that expected of a well-functioning n-channel TTFT. Figure 5.7a indicates the Fermi level energy separation with respect to the bottom of the conduction band to be ~0.15-0.30 eV, as calculated assuming an electron relative density-of-state effective mass of 0.3 and a channel carrier density of 10^{13}-10^{16} cm^{-3}. Such a low range of carrier concentration ensures that the channel layer is highly insulating, as required for a properly functioning TTFT. The conduction band curvature is negative in Fig. 5.7b, consistent with a build-up of negative electron accumulation layer charge which is localized very near the insulator-channel interface, whereas it is positive in Fig. 5.7c, indicating the existence of positive depletion charge which extends across most of the thin (~10-80 nm) channel layer.

The inversion condition, in which there is a build-up of minority carrier holes very near to the channel-insulator interface, is noticeably absent from Fig. 5.7. This is intentional, since inversion is not relevant in the operation of a MIS capacitor employing a visibly transparent wide band gap semiconductor.

To confirm that inversion is indeed not relevant in a transparent MIS capacitor, recognize that the rate of minority carrier generation is given by n_i/τ_G and $n_i s_g$, for bulk and surface generation, respectively, where n_i is the intrinsic carrier concentration, τ_G is the generation lifetime, and s_g is the surface generation velocity (Schroder 2006). Thus, the minority carrier generation rate depends on the channel layer intrinsic carrier concentration. For a semiconductor with a band gap of 3 eV and electron & hole relative density-of-state effective masses of 0.3 and 0.5, respectively, the intrinsic carrier concentration is extraordinarily small, $n_i \sim 10^{-8}$ cm^{-3}. Recognizing that n_i(silicon) ~ 10^{10} cm^{-3}, the wide band gap minority carrier generation rate is expected to be ~18 orders of magnitude less than that of silicon! Moreover, since a wide band gap semiconductor as required for transparency, it requires ~2.5-3 V of surface potential modulation from flat-band to inversion compared to ~0.7-1 V for silicon. Additionally, surface potential modulation in a wide band gap semiconductor requires the

depletion of filled deep level traps and band tail states prior to reaching inversion. For all of these reasons, inversion does not appear to be relevant for transparent-electronics-relevant MIS capacitors.

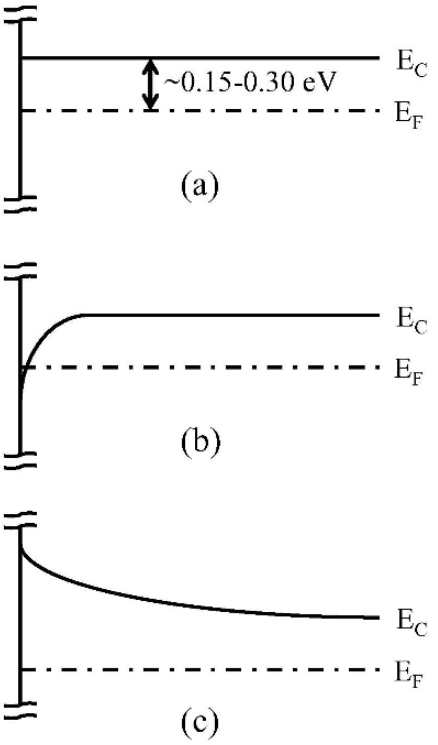

Fig. 5.7. Energy band diagrams (valence bands not shown) for (a) flat-band, (b) accumulation, and (c) depletion for an n-type semiconductor with a doping concentration typical for that expected of a TTFT channel layer, i.e., ~10^{13}-10^{16} cm^{-3}. Note that inversion is not shown, since this situation is not relevant for a TTFT.

Returning to the generic operation of a MIS capacitor in the context of transparent electronics, recognize that in a transparent MIS capacitor the 'metal' is actually a highly conductive TCO such as ITO. A voltage of appropriate polarity is applied to the 'metal' gate to either create an accumulation channel (+ voltage for an n-TTFT) or to deplete the channel (- voltage for an n-TTFT) in order to get rid of the build-up of the accumulated electrons at the insulator-channel interface. Looking ahead to the operation of a TTFT, accumulation (depletion) layer formation corresponds to turning the TTFT on (off).

Table 5.10 is a summary of MIS device equations which we believe to be relevant to transparent electronics. The first two equations simply specify the capacitance density of the insulator and the semiconductor. The third and fourth equations define normalized charge-centroid factors for charge distributed throughout the insulator and semiconductor, respectively. Various formulations of the third equation are sometimes used in discussions of mobile ion charge in the context of the Si-SiO_2 interface (Pierret 1996; Schroder 2006), since this charge is, in general, distributed throughout the oxide. We generalize this equation to account for an arbitrary number of types of charge, which could be distributed within the insulator (γ_i^{INS}), within the semiconductor (γ_j^{SEMI}; this formulation implies that the semiconductor behaves as an insulator, which constitutes a zero-order approximation for a highly insulating channel layer), or at the semiconductor interface, in which case $\gamma_i^{INS} = 1$ and $\gamma_j^{SEMI} = 0$.

The utility of using a normalized charge-centroid factor in such a formulation arises from the fact that many different types of charge can be easily accounted for in a very simple manner, without having to worry about the complication of charge distribution within the MIS capacitor. As a point-of-reference, Si-SiO_2 charges typically considered are fixed oxide, oxide-trapped, mobile ion, interface state charge, as well as implanted charge for threshold adjustment (Pierret 1996; Schroder 2006).

The flat-band voltage equation included in Table 5.10 is useful to the extent with which the metal-semiconductor work function difference and relevant charges and their spatial distribution are known. For device simulation purposes, all of the required information may be assumed, so that this equation is precise and quite useful. However, the inverse problem of unambiguously deducing information about the metal-semiconductor work function and charges and their distribution from a measurement of V_{FB} is quite hopeless, unless more is known about the MIS capacitor than is available from this single measurement.

If a TTFT actually operated in an ideal, one-dimensional manner, V_{FB} as specified in Table 5.10 would correspond to the TTFT turn-on voltage, V_{ON}, since electron accumulation and the onset of drain current would begin as soon as the applied gate voltage is sufficient to move the surface potential beyond flat-band. [Actually, this is only true for a well-functioning TTFT in which the channel layer has a very low carrier concentration. If the channel carrier concentration is not sufficiently low, additional gate voltage is required in order to deplete electrons from the bulk portion of

the channel. Such a TTFT will operate in depletion-mode, rather than in enhancement-mode.] In fact, V_{FB} differs from V_{ON} since TTFT operation is two-dimensional and also involves other kinds of non-idealities such as channel layer and interface trap filling. Thus, we typically prefer an empirical definition of V_{ON} as the onset of drain current as measured from the $\log(I_D)$- V_{GS} transfer characteristics of a TTFT (Hoffman 2004), as explained in more detail in Section 5.3.1.

For elucidation of many aspects of TTFT device physics operation, we have found the *discrete trap model* to be extremely useful. This model was originally introduced by Sze (Sze 1969), although we have extended it somewhat (Hong et al. 2007) and herein introduce further extensions and modifications of it.

The first V_{ON} entry included in Table 5.10, in which the trap is assumed to be acceptor-like, i.e., negatively charged if the trap is occupied with an electron and neutral if it is not occupied with an electron (as indicated at the end of the second column of the acceptor-trap V_{ON} entry of Table 5.11), corresponds to Sze's original formulation. The origin of this equation is recognizable as Q = CV when Q is identified as equal to $-q(n_{co}+n_{to})$, where n_{co} and n_{to} are the equilibrium (zero-bias) density of conduction band and occupied trap states, respectively. Note that in this acceptor trap model, both delocalized electronic charge (n_{co}) and localized trapped charge (n_{to}) are negative quantities, since they constitute negative charge. A consequence of this single polarity situation is that the acceptor-trap turn-on voltage is constrained to be negative or zero, i.e., $V_{ON} \leq 0$ V, so that this model by itself (i.e., without a flat-band voltage correction, as introduced later in Section 5.3.2) can only account for depletion-mode TTFT behavior. An implicit assumption of the discrete trap model is that both the delocalized electronic charge and the trapped charge are located directly at the insulator-semiconductor interface; thus, this model is, in reality, a discrete interface trap model.

Table 5.10. A summary of transparent-electronics-relevant MIS capacitor device equations.

Quantity Assessed	Equation
Insulator capacitance per unit area	$C_G = \frac{\varepsilon_G}{t_G}$
Semiconductor capacitance per unit area	$C_S = \frac{\varepsilon_S}{h}$
Normalized insulator charge-centroid factor	$\gamma_i^{INS} = \frac{1}{t_G Q_i}\int_0^{t_G} x\rho_i(x)dx$
Normalized semiconductor charge-centroid factor	$\gamma_j^{SEMI} = \frac{1}{hQ_j}\int_{t_G}^{t_G+h} (x-t_G)\rho_j(x)dx$
Flat-band voltage	$V_{FB} = \phi_{MS} - \sum_i \frac{\gamma_i^{INS} Q_i}{C_G} - \sum_j Q_j\left(\frac{1}{C_G} + \frac{\gamma_j^{SEMI}}{C_S}\right)$
Turn-on voltage (discrete acceptor trap model)	$V_{ON} = \frac{-q}{C_G}(n_{co} + n_{to}) \quad \frac{-}{0}$
Turn-on voltage (discrete donor trap model)	$V_{ON} = \frac{-q}{C_G}(n_{co} - p_{to}) \quad \frac{0}{+}$
Threshold voltage (discrete trap model; valid for acceptor & donor traps)	$V_T = \frac{q}{C_G}\left[(N_t - n_{to}) + (n_1 - n_{co})\right]$

ε_G = gate insulator dielectric constant (F cm^{-1})
t_G = gate insulator thickness (cm)
ε_S = semiconductor dielectric constant (F cm^{-1})
h = semiconductor thickness (cm)
Q_i = ith contribution to charge density within insulator (C cm^{-2})
$\rho_i(x)$ = ith contribution to charge density distributed within insulator (C cm^{-3})
x = distance from metal-insulator interface, i.e., x = 0 (cm)
Q_j = jth contribution to charge density within insulator (C cm^{-2})
$\rho_j(x)$ = jth contribution to charge density within semiconductor (C cm^{-3})
ϕ_{MS} = 'metal'-semiconductor work function difference (V)
DISCRETE TRAP MODEL PARAMETERS:
q = electronic charge (C)
n_{co} = equilibrium (zero-bias) sheet conduction band density (cm^{-2})
n_{to} = equilibrium sheet density of occupied traps (acceptor trap model) (cm^{-2})
p_{to} = equilibrium sheet density of empty traps (donor trap model) (cm^{-2})
N_t = trap sheet density (cm^{-2})
n_1 = sheet conduction band density when $E_F = E_T$ (E_T = trap energy) (cm^{-2})
n_{co}, n_{to}, N_t, n_1 = interface quantities

We have reformulated the discrete trap model by assuming that the trap may be donor-like. This leads to an identification of Q in the Q=CV equation as being equal to $-q(n_{co}-p_{to})$, where p_{to} is equal to the equilibrium (zero-bias) sheet density of empty (and hence positively charged) trap states. The primary advantage of this donor trap model compared to that of the acceptor trap model is the lack of constraint on V_{ON} such that it can be either negative, zero, or positive, without having to introduce the flat-band voltage correction discussed in Section 5.3.2. Thus, both depletion- and enhancement-mode TTFTs may be directly described using the discrete donor trap model.

The final equation entry in Table 5.10 specifies a threshold voltage, V_T, for the discrete trap model. This equation is equally applicable to either an acceptor- or a donor-like trap. In the context of the discrete trap model, note that the term $[q/C_G\ (N_t-n_{to})]$ corresponds to the gate voltage required for complete trap filling, while $[q/C_G\ (n_1-n_{co})]$ is equal to the corresponding conduction band state filling voltage, when the Fermi-level is equal to the trap energy, so that all of the traps are essentially filled.

The utility of the discrete trap model equations, as well as the other equations included in Table 5.11 is best appreciated in the context of a discussion of TTFT operation, a topic addressed in Section 5.3.2.

Certain aspects of MIS capacitor theory are employed in Section 6.2.2, relating to the passivation of TTFT channel layers.

5.4 Transparent thin-film transistors (TTFTs)

TTFTs constitute the heart of transparent electronics. Thus, this topic is presented in more detail than any of the other topics treated in this chapter. The first two sections focus on ideal and non-ideal behavior of n-channel TTFTs. Next, n-channel TTFT stability is considered. Finally, issues related to alternative device structures – double-gate TTFTs and the realization of p-channel TTFTs - are discussed.

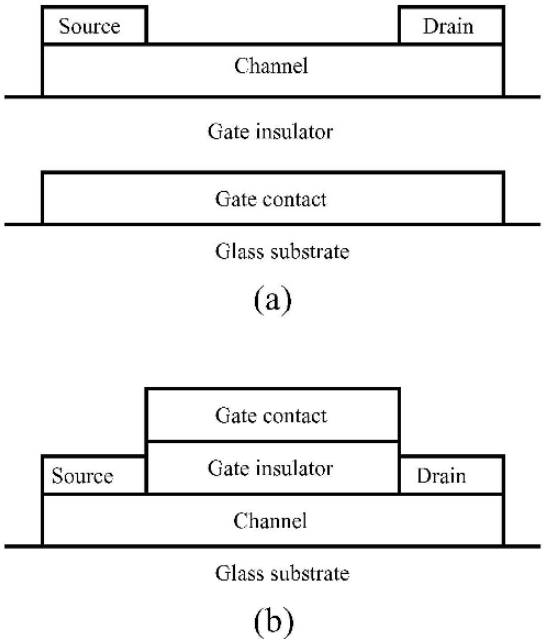

Fig. 5.8. Two possible transparent thin-film transistor (TTFT) device structures, (a) a staggered, bottom-gate, and (b) a coplanar, top-gate.

5.4.1 Ideal behavior

Figure 5.8 illustrates two of four possible TTFT device structures. The first one, considered in Fig. 5.8a, is denoted as a staggered, bottom-gate since source-drain and gate contacts are located at the top and bottom of the device, respectively. Figure 5.8b shows a coplanar, top-gate structure in which the source-drain and the gate are all positioned on the top side of the TTFT. The remaining two TTFT device structures, not shown, are the staggered, top-gate and coplanar, bottom-gate configurations. Although in a conventional TFT, the source, drain, and gate contact materials would be metals, a highly conductive TCO, such as ITO, is used in a TTFT. Additionally, while the channel layer of a conventional TFT employs a narrow band gap, opaque semiconductor, a highly insulating, wide band gap transparent semiconductor is used in a TTFT.

Ideal operation of an n-channel TTFT is described as follows.

With the source grounded, a positive voltage is applied to the drain in order to attract electrons from the source to the drain. The amount of drain current, I_D, which flows from the source to the drain depends upon whether or not an electron accumulation layer exists at the channel-insulator interface. No drain current flows if the gate-source voltage, V_{GS}, is less than the turn-on voltage, V_{ON}, since electrons are not present in the channel. This situation is indicated in Fig. 5.9a. Thus, it is the low carrier concentration nature of the channel which holds off the flow of drain current between the source and the drain for V_{GS}'s below V_{ON}.

If a gate voltage, V_{GS}, greater than V_{ON} is applied while a positive voltage exists at the drain, i.e., if V_{DS} is positive, drain current flows, as indicated in Fig. 5.9b. Physically, electrons are injected from the source into the gate-bias-induced electron accumulation layer channel, are transported across this low-resistance accumulation layer, and are extracted at the drain contact. This electron transport process corresponds to the flow of drain current in the opposite direction, from the drain to the source. The magnitude of drain current flowing depends on the gate overvoltage, i.e., on V_{GS}-V_{ON}, which determines the accumulation layer sheet charge density, and also on the magnitude of the drain voltage, which establishes the electric-field aided drift condition along the channel, from the source to the drain. For small V_{DS}'s compared to the gate overvoltage (i.e., for $V_{DS}<<V_{GS}$-V_{ON}), drain current flow in the channel is describable using Ohm's law, i.e., $I_D = V_{DS}/R_C(V_{GS})$, where $R_C(V_{GS})$ is the resistance of the channel, indicating that electron transport across the channel may be modeled as simply resistive. In fact, the channel resistance is indicated in Ohm's law in the functional form $R_C(V_{GS})$ since the channel resistance depends on the accumulation layer sheet charge density, which is controlled by V_{GS}.

As the magnitude of this applied positive drain voltage increases so that V_{DS} is no longer negligible compared to the overvoltage (V_{GS}-V_{ON}), I_D is no longer Ohmic with respect to V_{DS}, but, rather, becomes sublinear and eventually saturates when channel pinch-off occurs at $V_{DS}\equiv V_{DSAT}=V_{GS}$-$V_{ON}$.

Pinch-off may be understood quantitatively by recognizing that the electron accumulation layer sheet charge density is given by $Q_n(y)=C_G[V(y)$-$V_{ON}]$, where V(y) is the channel-insulator interfacial voltage drop along the channel from the source to the drain, with y=0 and y=L corresponding

to distances along the channel at the edge of the source and the edge of the drain, respectively. At the drain edge of the channel, $Q_n(L)=C_G[V_{GS}-V_{DS}-V_{ON}]$. Thus, the accumulation layer sheet charge density is equal to zero at y=L, and the channel is therefore depleted or 'pinched off', when the term in the square brackets goes to zero, leading to the pinch-off relationship as specified by the first entry in Table 5.11. This nonlinear, pre-pinch-off to saturated, post-pinch-off situation is sketched in Fig. 5.9c, attempts to capture both the drain voltage-induced elimination of the electron accumulation layer channel near the drain-end of the channel, and the inherently 2-dimensional nature of the TTFT electric field near the drain in this regime of device operation.

A quantitative formulation of ideal TTFT operation is given according to square-law theory (Borkan and Weimer 1963; Tickle 1969; Hong et al. 2007), as summarized in Table 5.11. Note that the linear or Ohmic regime, as indicated in Fig. 5.9b, corresponds to the pre-pinch-off limit in which $V_{DS}<<V_{GS}-V_{ON}$ so that $I_D\approx(W/L)\mu C_G(V_{GS}-V_{ON})V_{DS}$, which means that $R_C(V_{GS})=(W/L)\mu C_G(V_{GS}-V_{ON})$. Ideal aspects of square-law theory include the absence of subthreshold current (i.e., the subthreshold swing, S=0) and hard saturation of the drain current characteristics (i.e., in saturation, $dI_D/dV_{DS} = 0$). Further aspects of ideal, square-law theory are developed in Section 5.3.2, in the context of establishing limits to non-ideal TTFT behavior.

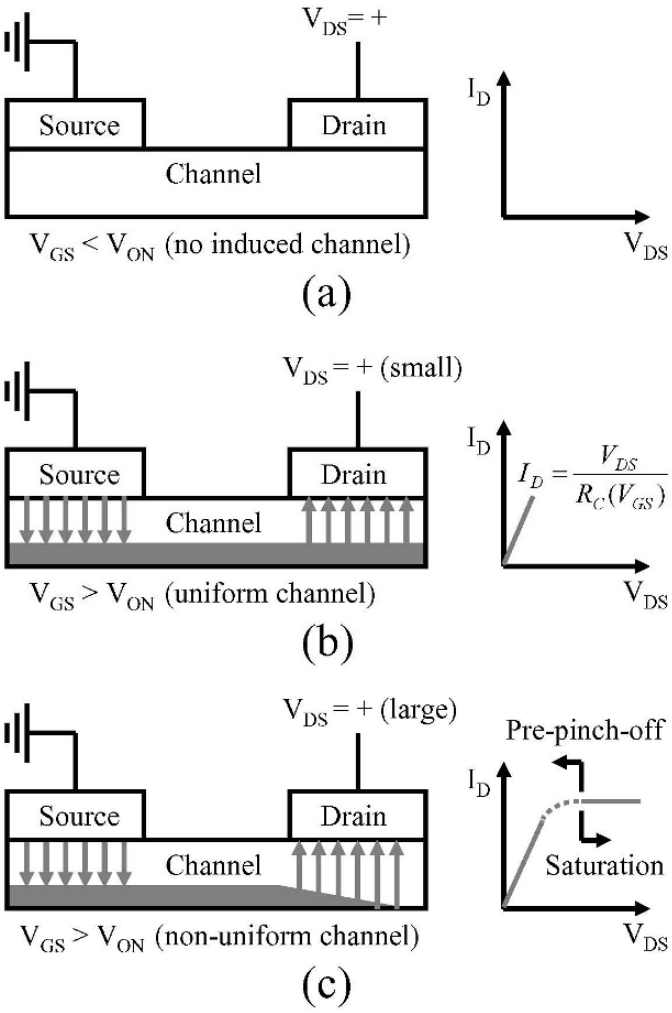

Fig. 5.9. Ideal n-channel transparent thin-film transistor (TTFT) operation. (a) Cut-off. Zero drain current (I_D=0) occurs in cut-off, which is defined by $V_{GS}<V_{ON}$, and corresponds to a situation in which no electron accumulation layer exists at the channel-gate insulator interface. (b) Linear, pre-pinch-off. I_D is described by Ohm's law [$I_D=V_{DS}/R_C(V_{GS})$] at low V_{DS}'s [$V_{DS}<<V_{GS}-V_{ON}$], corresponding to the formation of a uniform electron accumulation layer at the channel-gate insulator interface from the source to the drain. (c) Nonlinear, pre-pinch-off and, post-pinch-off, saturation. I_D becomes sublinear with respect to V_{DS} and then saturates when $V_{DS}\equiv V_{DSAT}=V_{GS}-V_{ON}$ because of the depletion or 'pinch-off' of the electron accumulation layer at the channel-gate insulator interface near the drain. V_{DSAT} defines the boundary between pre-pinch-off and post-pinch-off or saturation.

Table 5.11. A summary of ideal, square-law theory TTFT device equations.

Quantity Assessed	Equation
Pinch-off condition (V)	$V_{DSAT} = V_{GS} - V_{ON}$
Drain current (A)	$I_D = 0$ (cut-off; $V_{GS}<V_{ON}$) $I_D = \frac{W}{L}\mu C_G\left[(V_{GS}-V_{ON})V_{DS} - \frac{V_{DS}^2}{2}\right]$ (pre-pinch-off; $V_{GS}\geq V_{ON}$, $V_{DS}\leq V_{DSAT}$) $I_D \equiv I_{DSAT} = \frac{W}{2L}\mu C_G(V_{GS}-V_{ON})^2$ (post-pinch-off or saturation; $V_{GS}\geq V_{ON}$, $V_{DS}>V_{DSAT}$)

V_{DSAT} = drain-source voltage defining the onset of saturation (V)
V_{GS} = gate-source voltage (V)
V_{ON} = turn-on voltage (V)
W = gate width (μm)
L = gate length (μm)
μ = channel mobility ($cm^2\ V^{-1}s^{-1}$)
C_G = gate capacitance density ($F\ cm^{-2}$)
V_{DS} = drain-source voltage (V)
I_{DSAT} = saturation current (A)

5.4.2 Non-ideal behavior

The *discrete trap model* (Sze 1969; Hong et al. 2007), as introduced in Section 5.2.4 in the context of the MIS capacitor, is found to be useful for the elucidation of certain types of TTFT non-ideality. A summary of the device equations defining this non-ideal model are given in Table 5.12 for both acceptor-like and donor-like trap cases. The donor-trap model is sometimes preferred since both depletion- and enhancement-mode TTFTs may be described in a natural manner using this model, without having to invoke a flat-band correction. Alternatively, the acceptor-trap model is able to account for certain $\log(I_D)$-V_{DS} transfer curve non-idealities sometimes witnessed in poorly-performing TTFTs, as discussed in the following.

Table 5.12. A summary of non-ideal, discrete trap model TTFT device equations.

Quantity Assessed	Equation
Turn-on voltage (V)	$V_{ON} = \frac{-q}{C_G}\left(n_{co} + n_{to}\right) + V_{FB}$ (acceptor trap) $\frac{-}{0}$ $V_{ON} = \frac{-q}{C_G}\left(n_{co} - p_{to}\right) + V_{FB}$ (donor trap) $\frac{0}{+}$
Threshold voltage (V)	$V_T = \frac{q}{C_G}\left[\left(N_t - n_{to}\right) + \left(n_1 - n_{co}\right)\right] + V_{FB}$ (acceptor or donor trap)
Pinch-off condition (V)	$V_{DSAT} = V_{GS} - V_{ON}$ (acceptor trap) $V_{DSAT} = V_{GS} - V_{ON} + V_t$ (donor trap)
Drain current (A)	$I_D = 0$ (cut-off; $V_{GS}<V_{ON}$) $I_D = \frac{W}{L}\mu C_G\left[\frac{1}{2}aV_{DS} - \frac{1}{4}{V_{DS}}^2 + \frac{1}{4}\left(V_{DS} - a - \frac{c}{2}\right)C_1 + \left(V_t V_1\right)\ln\left(\frac{C_2}{C_3}\right) + \frac{1}{4}\left(a + \frac{c}{2}\right)\sqrt{a^2 + bc}\right]$ (pre-pinch-off; $V_{GS}\geq V_{ON}$, $V_{DS}\leq V_{DSAT}$) $I_D = I_{DSAT} \equiv \frac{W}{L}\mu C_G\left[\frac{1}{2}aV_{DSAT} - \frac{1}{4}{V_{DSAT}}^2 + \frac{1}{4}\left(V_t^2 - V_1^2\right) + \left(V_t V_1\right)\ln\left(\frac{4V_t}{C_3}\right) + \frac{1}{4}\left(a + \frac{c}{2}\right)\sqrt{a^2 + bc}\right]$ (post-pinch-off or saturation; $V_{GS}\geq V_{ON}$, $V_{DS}>V_{DSAT}$)

Table 5.12 (Continued).

Quantity Assessed	Equation
Model constants	$V_t = \frac{qN_t}{C_G},\ V_1 = \frac{qn_1}{C_G}$ $a = V_{GS} - V_t - V_{ON} - V_1$ (acceptor model) $a = V_{GS} - V_{ON} - V_1$ (donor model) $b = V_{GS} - V_{ON}$ (acceptor model) $b = V_{GS} + V_t - V_{ON}$ (donor model) $c = 4V_1$ (acceptor or donor model) $C_1 = \sqrt{\left(a - V_{DS}{}^2\right) + c\left(b - V_{DS}\right)}$ $C_2 = -2a - c + 2V_{DS} + 2C_1$ $C_3 = -2a - c + 2\sqrt{a^2 + bc}$

q = electronic charge (C)
C_G = gate capacitance density (F cm^{-2})
n_{co} = equilibrium (zero-bias) conduction band density (cm^{-2})
n_{to} = equilibrium density of occupied traps (acceptor trap model) (cm^{-2})
p_{to} = equilibrium density of empty traps (donor trap model) (cm^{-2})
N_t = trap density (cm^{-2})
n_1 = conduction band density when $E_F = E_T$ (E_T = trap energy) (cm^{-2})
V_{FB} = flat-band voltage (V)
V_{GS} = gate-source voltage (V)
V_{DS} = drain-source voltage (V)
V_{DSAT} = drain-source voltage defining the onset of saturation (V)
I_{DSAT} = saturation current (A)
W = gate width (μm)
L = gate length (μm)
μ = channel mobility (cm^2 V^{-1}s^{-1})
V_t = equivalent trap voltage (V)
V_1 = equivalent conduction band density voltage when $E_F = E_T$ (V)

Figure 5.10 presents a comparison of log(I_D)-V_{GS} transfer curves simulated using the discrete donor trap model as a function of trap density. An ideal transfer curve is also included in this figure, which is generated using the square-law model of Section 5.3.1. With increasing trap density, V_{ON} shifts to a higher V_{GS}. Additionally, I_D at a given V_{GS} overvoltage is somewhat reduced, such that a I_D-V_{GS} curve progressively smears out with increasing trap density. These trends make intuitive sense, since trap filling modifies the onset of I_D and retards the rate at which I_D increases with respect to increasing V_{GS}.

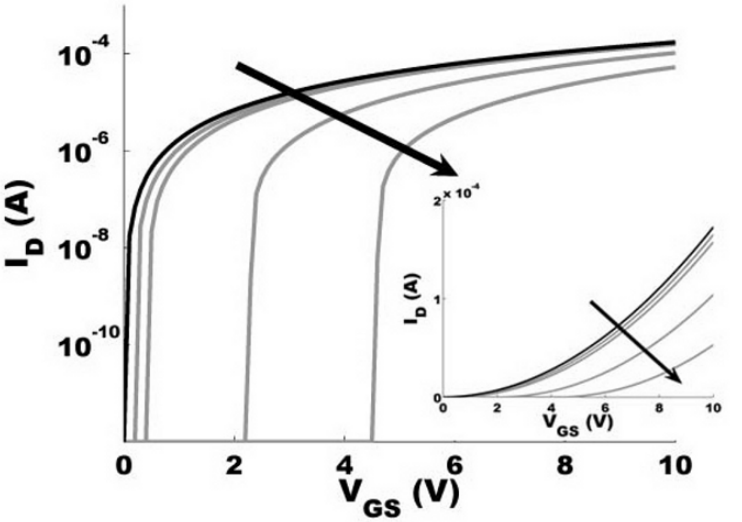

Fig. 5.10. Log(I_D)-V_{GS} transfer curve comparison between transparent thin-film transistor (TTFT) simulations at different trap densities. The arrow indicates the direction of increasing trap density. The top curve (dark) is generated using the ideal, square-law model of Section 5.3.1. All of the other curves are obtained using the discrete, donor-trap model summarized in Table 5.12, using trap sheet densities, $N_t = 10^{10}$, 5 X 10^{10}, 10^{11}, 5 X 10^{11}, and 10^{12} cm^{-2}. Corresponding I_D-V_{GS} curves are shown in the inset. For the ideal, square-law model, $V_{ON} = 0$ V. For both the ideal and non-ideal model simulations, $V_{DS} = 40$ V, (W/L) = 10, $\mu = 10$ cm^2/V-s, and $C_G = 34.5$ nF cm^{-2} (corresponding to 100 nm of SiO_2). For the non-ideal model simulations, E_C-$E_T = 0.15$ eV, $n_{co} = 10^8$ cm^{-2}, $m^*/m_o = 0.3$, and T = 300 K.

Two other aspects of Fig. 5.10 merit comment. First, note that the subthreshold drain current characteristics just beyond V_{ON} are exceedingly steep, implying that the subthreshold swing, S, is extremely small. This is a limitation of the discrete trap model, and is not representative of a real TTFT. Second, since a simulated log(I_D)-V_{GS} transfer curve has an infinitely small current for a V_{GS} infinitesimally above V_{ON}, the simulated drain current on-to-off ratio, I_D^{ON-OFF}, is also infinite. Both of these model limitation issues are addressed in the following discussion.

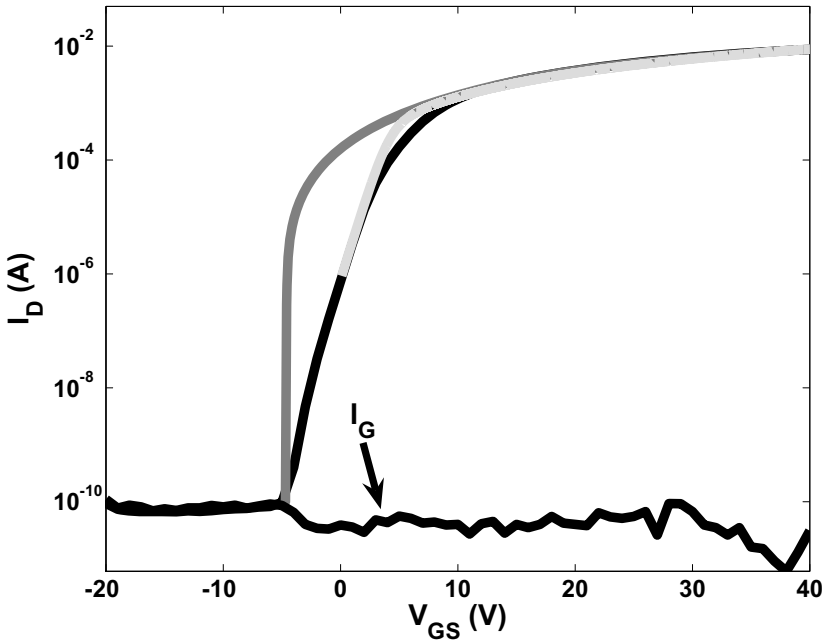

Fig. 5.11. Log(I_D)-V_{GS} transfer curve (dark) and log(I_G)-V_{GS} leakage curve for a transparent thin-film transistor (TTFT) with a 80 nm thick zinc tin oxide (Zn:Sn = 2:1) channel layer deposited by rf magnetron sputtering and subjected to a post-deposition furnace anneal at 600 ºC. The gray and whitish log(I_D)-V_{GS} transfer curves are simulated fits to the experimental data using, respectively, (i) the discrete, donor-trap model and (ii) the ideal, square-law model in conjunction with the subthreshold current augmentation procedure of Table 5.13 and mobility degradation of Eq. 5.8. The inset shows a comparison of measured (dark) and simulated (gray & light-gray) I_D-V_{GS} curves. The material, device structure, and operating parameters used in this simulation are $m^*/m_o = 0.3$, (W/L) = 5, $C_G = 60$ nF cm^{-2} (corresponding to 220 nm of ATO), $V_{DS} = 40$ V, and T = 300 K. The fitting parameters used in the discrete trap simulation are $\mu = 38$ cm^2/V-s, $N_t < 10^{13}$ cm^{-2}, E_C-$E_T = 0.2$ eV, and $n_{co} = 2 \times 10^{12}$ cm^{-2}. The fitting parameters used in the ideal, square-law with subthreshold current augmentation procedure simulation are $V_{ON} = -2.6$ V, m = 1, and $D_{IT} = 2.3 \times 10^{11}$ $cm^{-2}eV^{-1}$, $\mu = 75$ cm^2/V-s, and $\theta = 0.03$ V^{-1}, where θ is the interface degradation factor (see Eq. 5.8).

A measured log(I_D)-V_{GS} transfer curve and a log(I_G)-V_{GS} leakage curve are given in Fig. 5.11. In contrast to the simulation indicated in Fig. 5.10, V_{ON} and I_D^{ON-OFF} are unambiguously determined to be -5 V and ~10^8, respectively. These two quantities are precisely established by the gate leak-

age current, which at very low currents may also be partially determined by the instrumentation noise floor. Thus, real-world leakage-noise considerations, which are not readily independently calculable via simulation, are largely responsible for establishing V_{ON} and I_D^{ON-OFF} in an actual TTFT.

Two simulations are undertaken in an attempt to fit the measured $\log(I_D)$-V_{GS} transfer curve shown in Fig. 5.11.

The gray curve indicated in Fig. 5.11 is obtained using the discrete, donor-trap model. The equilibrium conduction band density, n_{co}, which sets the equilibrium Fermi level position is found to be the critical parameter for fitting V_{ON}, whereas the channel mobility, μ, is key for obtaining a good fit to the maximum current. For this depletion-mode device, the magnitude of the total trap density, N_t, is to a large extent irrelevant in establishing V_{ON}, as long as it is kept below 10^{13} cm^{-2}. Additionally, the trap energy depth is not critical. The most striking aspect of the discrete donor trap simulation shown in Fig. 5.11 is that it is completely inadequate in describing the subthreshold behavior of a real TTFT, even though it models the beyond-threshold portion of the measured data quite well.

In contrast, the whitish line fit to the measured data of Fig. 5.11 is a significant improvement, compared to the discrete trap model simulation. The whitish line simulation is generated using the subthreshold current augmentation procedure summarized in Table 5.13, with a constant density of subthreshold traps, in conjunction with the ideal, square-law model of Table 5.11. In addition to accurately modeling the above-threshold portion of the curve, a section of the subthreshold trend can also be accounted for through the inclusion of a trap with a uniform density that turns on at V_{ON} and essentially turns off above threshold when the ideal, square-law model contribution becomes dominant compared to the subthreshold current contribution. In this simulation, the turn-on is specified to occur at V_{ON} = -2.5 V instead of at the measured value of -5 V. This occurs because only a portion of the subthreshold slope can be fit, using a uniform trap density, and it is the most linear portion of the subthreshold trend which is fit. Two other model parameters, μ = 75 $cm^2/V\text{-}s$ and $D_{IT} = 2.3 \times 10^{11}$ $cm^{-2}eV^{-1}$, are used to fit the maximum current and the most linear portion of the subthreshold slope, respectively. Although this model cannot accurately reproduce the entire measured curve, the fit is considered quite good, given that only three adjustable parameters are employed. A better fit would require the use of a nonuniform distribution of traps.

Table 5.13. A summary of device equations constituting a subthreshold current augmentation procedure, suitable for use in conjunction with either an ideal or a non-ideal TTFT device model (Jacunski et al. 1999; Nathan et al. 2004). Subthreshold current is calculated assuming a uniform density or a subthreshold uniform density of traps. In either case, the lowest energy at which the trap density is assumed to exist corresponds to that of the turn-on voltage, V_{ON}.

Quantity Assessed	Equation
Interface capacitance density (F cm^{-2})	$C_{IT} = \frac{q^2 D_{IT}}{k_B T}$
Subthreshold current (A)	$I_{D,SUB} = \frac{W}{L}\mu C_G \left(\frac{k_B T}{q}\right)^2 e^{\frac{q(V_{GS}-V_{ON})}{\left(1+\frac{C_{IT}}{C_G}\right)k_B T}} \times \left[1 - e^{\frac{-qV_{DS}}{k_B T}}\right]$ (pre-pinch-off; $V_{GS} \geq V_{ON}$, $V_{DS} \leq V_{DSAT}$)
	$I_D = 0$ (cut-off; $V_{GS} < V_{ON}$)
Drain current (A)	
$m = 1$: uniform subthreshold trap density	$(I_D)^{-1} = (I_{D,SUB})^{-1} + \frac{(I_{D,PPO})^{-1}}{m}$ (pre-pinch-off; $V_{GS} \geq V_{ON}$, $V_{DS} \leq V_{DSAT}$)
$m = 1 + \frac{C_{IT}}{C_G}$: uniform trap density	$I_D = I_{DSAT}$ (saturation; $V_{GS} \geq V_{ON}$, $V_{DS} > V_{DSAT}$)

D_{IT} = interface state density (# cm^{-2})
q = electronic charge (C)
W = gate width (μm)
L = gate length (μm)
μ = channel mobility (cm^2 V^{-1}s^{-1})
C_G = gate capacitance density (F cm^{-2})
k_B = Boltzmann's constant (J/K)
T = temperature (K)
V_{GS} = gate-source voltage (V)
V_{ON} = turn-on voltage (V)
V_{DS} = drain-source voltage (V)
V_{DSAT} = drain-source voltage defining the onset of saturation (V)
$I_{D,PPO}$ = pre-pinch-off current (A)
I_{DSAT} = saturation current (A)

In contrast to Fig. 5.10, which is generated using the discrete, donor-trap model, a kink is present at high trap densities in the $\log(I_D)$-V_{DS} transfer curves shown in Fig. 5.12, which are simulated using the discrete, acceptor-trap model. Since poorly performing TTFTs occasionally exhibit $\log(I_D)$-V_{DS} transfer curves possessing a kink, the purpose of the simulations illustrated in Fig. 5.10 is to elucidate the origin of such kinks.

The trend present in Fig. 5.12 arises as follows. First, consider the $N_t = 10^{13}$ cm^{-2} curve. The shape of this I_D curve with increasing V_{GS} between ~0 and ~40 V is determined, to a large extent, by the filling of trap states as the Fermi level in the channel is modulated towards the conduction band minimum. Most of these traps are filled when V_{GS} is equal to the threshold voltage, $V_T = 46$ V, so that the shape of the I_D curve beyond V_T is, to a large extent, established exclusively by the filling of conduction band states. The $N_t = 5 \text{ X } 10^{12}$ cm^{-2} curve also possesses a distinct kink, but it is now located at a lower V_{GS}, corresponding to $V_T = 23$ V. In contrast, the $N_t = 1 \text{ X } 10^{12}$ cm^{-2} curve does not have a kink, although its transfer curve is slightly distorted by a transition region centered approximately at the threshold voltage, $V_T = 4.7$ V. Finally, the $N_t = 1 \text{ X } 10^{11}$ cm^{-2} curve, in which $V_T = 0.5$ V, displays no kink or discernable trap-induced distortion of the transfer curve.

Thus, the kinks and other distortion present in the $\log(I_D)$-V_{GS} transfer curves shown in Fig. 5.12 originate from acceptor-trap filling. More precisely, according to the discrete, acceptor-trap model, as summarized in Table 5.12, it can be shown that $V_T - V_{ON} = V_t + V_1$, where V_t is the equivalent trap voltage corresponding to N_t and V_1 is the equivalent conduction band density voltage when $E_F = E_T$. This relationship is revealing since, it turns out, a kink is present in a $\log(I_D)$-V_{GS} transfer curve only when (i) $V_T - V_{ON}$ is appreciable, i.e., greater than ~10 V, and (ii) when it is also dominated by V_t, but not by V_1. In contrast, according to the discrete, donor-trap model, as summarized in Table 5.12, $V_T - V_{ON} = V_1$, which, it turns out, implies that $\log(I_D)$-V_{GS} transfer curves simulated using this model never exhibit a kink.

The fact that the discrete, acceptor-trap model yields $\log(I_D)$-V_{GS} transfer curves with kinks (when N_t is sufficiently large), whereas the discrete, donor trap model does not, appears to have important diagnostic implications related to the development of TTFT channel layers, since kinks are sometimes observed in the transfer curves of TTFTs with poorly performing channel layers. Although not inconceivable, it is unlikely that a 'bulk' (i.e. non-interface) trap in the uppermost portion of the band gap near to

the conduction band minimum would be acceptor-like. However, as discussed in Section 5.3.2 in conjunction with the charge neutrality level, E_{CNL}, acceptor-like behavior is expected for interface traps in the upper portion of the band gap above E_{CNL}. Therefore, in our TTFT channel layer developmental efforts, when we experimentally establish that there is a kink in a measured $\log(I_D)$-V_{GS} transfer curve, we tentatively conclude that this device possesses a high density of *interface* states, thus degrading its performance, and that the source of this interface state density must be identified and eliminated.

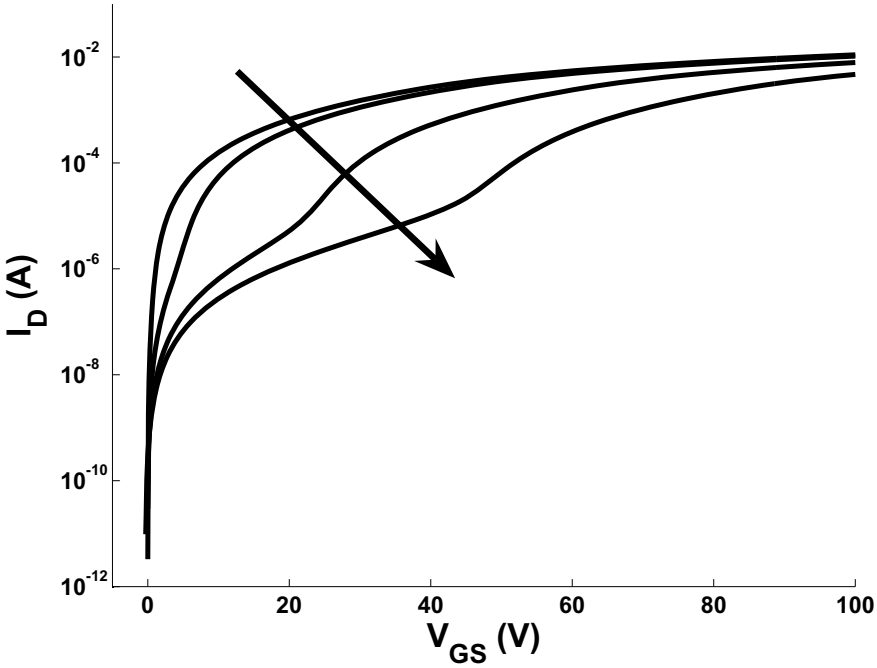

Fig. 5.12. $\text{Log}(I_D)$-V_{GS} transfer curve comparison between transparent thin-film transistor (TTFT) simulations at different trap densities. The arrow indicates the direction of increasing trap density. All curves are obtained using the discrete, acceptor-trap model summarized in Table 5.12, using trap sheet densities, $N_t = 10^{11}$, 10^{12}, 5 X 10^{12}, and 10^{13} cm^{-2}. For these simulations, V_{DS} = 40 V, (W/L) = 10, μ = 10 cm^2/V-s, and C_G = 34.5 nF cm^{-2} (corresponding to 100 nm of SiO_2), E_C-E_T = 0.15 eV, $n_{co} = 10^8$ cm^{-2}, m^*/m_o = 0.3, and T = 300 K.

In summary, the simulations shown in Figs. 5.10-12, clearly indicate that the non-idealities manifest in the $\log(I_D)$-V_{GS} transfer curves of real TTFTs are, to a large extent, a consequence of electron trapping. Physically, in these simulations, electrons are usually assumed to possess a con-

stant mobility when they occupy conduction band states, but are also subject to trapping, in which case a portion of the electron distribution injected into the channel is localized in traps, and thus not available to contribute to the current.

A different, but to a certain extent equivalent approach for handling certain non-ideal aspects of TTFT operation is to extract the channel mobility as a function of gate voltage [$\mu(V_{GS})$] from $I_D(V_{GS},V_{DS})$ data. As discussed in Section 2.2.2 and in reference (Hong et al. 2007), several different channel mobility extraction procedures are available. In the following discussion, we use Hoffman's average mobility [which physically corresponds to the *average* mobility of all of the carriers present in the channel (Hoffman 2004)], as specified by a slightly modified defining expression,

$$\mu_{AVG}(V_{GS}) = \underset{V_{DS}\to 0}{Lim}\left[\frac{G_d(V_{GS})}{\frac{W}{L}C_G\left(V_{GS}-V_{ON}\right)}\right], \tag{5.1}$$

where Eq. 5.1 differs superficially from the corresponding equation given in Table 2.2 since g_d (= dI_D/dV_{DS}) in Table 2.2 is replaced by G_d (= I_D/V_{DS}) in Eq. 5.1. In the limit of V_{DS} approaching zero, $g_d = G_d$, at least to the extent with which the device is in the linear regime of operation. The motivation for replacing g_d by G_d is associated with its computational convenience. In a similar manner, Hoffman's incremental mobility [which physically corresponds to the *incremental* mobility of carriers *added* to the channel as the gate voltage differentially increases in magnitude (Hoffman 2004)], is also specified by a slightly modified defining expression,

$$\mu_{INC}(V_{GS}) = \underset{V_{DS}\to 0}{Lim}\left[\frac{\frac{\partial G_d(V_{GS})}{\partial V_{GS}}}{\frac{W}{L}C_G}\right]. \tag{5.2}$$

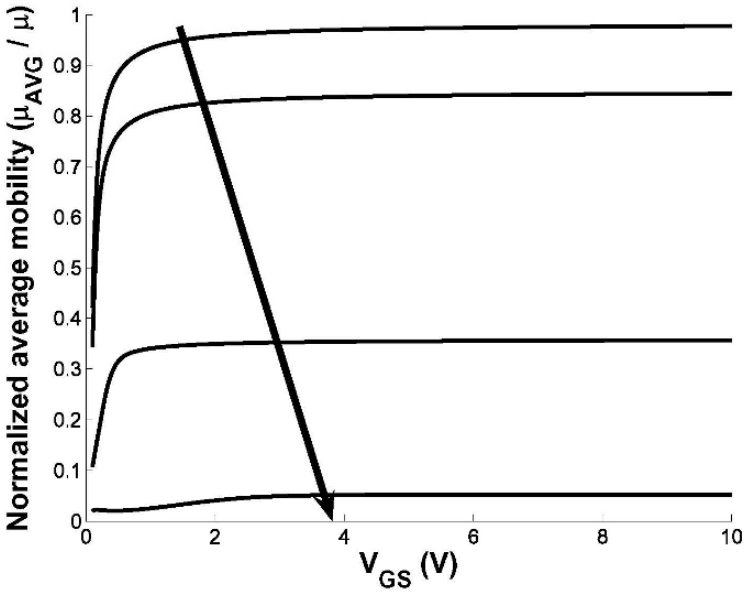

Fig. 5.13. Normalized average mobility as a function of gate-source voltage [i.e., $\mu_{AVG}(V_{GS})/\mu$, where μ is the simulation channel mobility] curve comparison between transparent thin-film transistor (TTFT) simulations at different trap densities. The arrow indicates the direction of increasing trap density, with $D^{IT} = 10^8$, 10^9, 10^{10}, 10^{11} $cm^{-2}eV^{-1}$ and $m = 1 + C_{IT}/C_G$ (i.e., a uniform trap density beyond the turn-on voltage). This simulation is performed using the subthreshold current augmentation procedure of Table 5.13 in conjunction with the ideal, square-law TTFT device model of Table 5.11. Other simulation parameters are $V_{DS} = 40$ V, $(W/L) = 10$, $\mu = 10$ $cm^2/V\text{-}s$, and $V_{ON} = 0$ V.

Figure 5.13 illustrates a set of simulated $\mu_{AVG}(V_{GS})$ curves for a TTFT having different trap densities. These curves are simulated using the subthreshold current augmentation procedure of Table 5.13 (assuming a uniform trap density beyond the turn-on voltage) in conjunction with the ideal, square-law model of Table 5.11. Several trends are demonstrated in this simulation. First, the relatively constant, almost-saturated value of mobility at larger V_{GS}'s is dramatically reduced with increasing trap density. Thus, this simulation confirms that electron trapping degrades the channel mobility in a TTFT. Second, if the trap density is low, only a small amount of overvoltage, i.e., V_{GS}-V_{ON}, is required to reach a 'saturated' value of the channel mobility. However, as the trap density increases, a larger overvoltage must be applied to reach mobility 'saturation (see the $D^{IT} = 10^{11}$ $cm^{-2}eV^{-1}$ curve) and the slope of the early part of the

mobility curve just above V_{ON} is less steep (see the $D^{IT} = 10^{10}$ $cm^{-2}eV^{-1}$ curve).

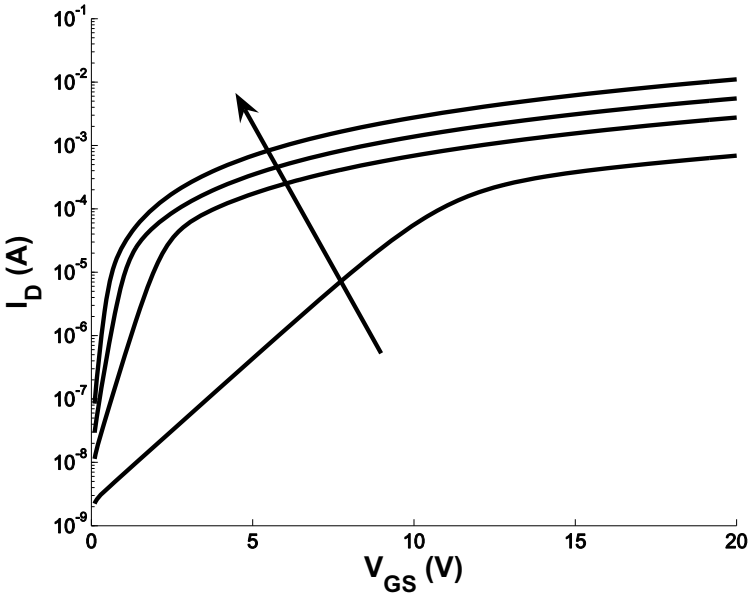

Fig. 5.14. $Log(I_D)$-V_{GS} transfer curve comparison between transparent thin-film transistor (TTFT) simulations at different gate insulator capacitance densities. The arrow indicates the direction of increasing gate capacitance density. The curve furthest to the right is for $C_G = 34.5$ nF cm^{-2} (corresponding to 100 nm of SiO_2). C_G is increased by a factor of 4X, 8X, and 16X, respectively, for the other curves shown. This simulation is performed using the subthreshold current augmentation procedure of Table 5.13 in conjunction with the ideal, square-law TTFT device model of Table 5.11. Other simulation parameters are $V_{DS} = 40$ V, (W/L) = 10, $\mu = 10$ cm^2/V-s, $V_{ON} = 0$ V, $D^{IT} = 2 \times 10^{11}$ $cm^{-2}eV^{-1}$, and m = 1 (i.e., a uniform subthreshold trap density).

Another aspect of electron trapping, and one strategy for coping with it, is captured in Figure 5.14, which presents a $log(I_D)$-V_{GS} transfer curve comparison between TTFTs which are simulated at different gate insulator capacitance densities. This simulation is performed using the subthreshold current augmentation procedure of Table 5.13 (assuming a uniform subthreshold trap density) in conjunction with the ideal, square-law TTFT device model of Table 5.11. This simulation clearly illustrates the advantage of using a high-k gate dielectric. The important point to note is that when a high capacitance density gate dielectric is used, the I_D subthreshold swing can be quite small, allowing the device to abruptly and strongly turn

on using very little overvoltage, even when the interface trap density is relatively large (D^{IT} = 2 X 10^{11} $cm^{-2}eV^{-1}$ for the case shown in Fig. 5.14). Thus, we believe that development of a robust, high-k dielectric is a very important goal for the future of transparent electronics, even though this will lead to challenges related to minimizing parasitic TTFT overlap capacitance.

Table 5.14. A summary of ideal and non-ideal TTFT issues and corresponding model parameters & considerations.

Issue	Model parameters & considerations
Ideal behavior	$\frac{W}{L}$, C_G, V_{ON}, μ
Non-ideal behavior	$\frac{W}{L}$, C_G, V_{ON}, μ(V_{GS}), S, R_S, R_D, R_{BULK}, $R_{SURFACE}$, R_d^{SAT}
Trapping	μ (V_{GS}), S
Interface roughness	μ(V_{GS})
Series resistance	R_S, R_D
Conductive channel	R_{BULK}, $R_{SURFACE}$, R_d^{SAT}
Channel length modulation	R_d^{SAT}
Gate leakage / noise floor	I_D^{ON-OFF}
Insulator leakage	R_{GS}, R_{GD}
Unpatterned channel, fringing current artifact	I_D & μ = overestimated

W = channel width
L = channel length (μm)
C_G = gate insulator capacitance density (F cm^{-2})
V_{ON} = turn-on voltage (V)
μ = channel mobility ($cm^2V^{-1}s^{-1}$)
V_{GS} = gate-source voltage (V)
V_{DS} = drain-source voltage (V)
S = subthreshold swing ($Vdecade^{-1}$)
R_S, R_D = source, drain series resistance (Ω)
R_{BULK}, $R_{SURFACE}$ = bulk, surface channel layer shunt resistance (Ω)
R_d^{SAT} = channel resistance in saturation = $\left[\left.\frac{\partial I_D}{\partial V_{DS}}\right|_{SAT}\right]^{-1}$ (Ω)
R_{GS}, R_{GD} = gate-source, gate-drain insulator leakage resistance (Ω)

Up to now, this explication of TTFT non-idealities has been facilitated exclusively by employing trap-based models to elucidate trapping-related non-idealities. Changing directions somewhat, Table 5.14 is offered as a focal point for initiating a comparison of ideal and non-ideal TTFT behavior, and also for then extending this discussion to other types of TTFT non-idealities.

The first entry in Table 5.14 involves a collection of ideal model parameters, i.e., (W/L), C_G, V_{ON}, μ. These four parameters, together with the defining equations included in Table 5.11, constitute a complete static or DC description of the electrical operation of an ideal TTFT. A convenient way to represent this model is to specify it in the functional form,

$$I_D(V_{GS}, V_{DS}; (W/L), C_G, V_{ON}, \mu), \tag{5.3}$$

where I_D is the dependent variable, V_{GS} & V_{DS} are independent variables, and (W/L), C_G, V_{ON}, μ are model parameters which need to be specified for a given TTFT before its behavior can be simulated using this mathematical model. From a device physics perspective, Eq. 5.3 is an appropriate model parameter formulation of the ideal model. However, from a circuit modeling-simulation perspective, Eq. 5.3 is unnecessarily complicated since this model may be equivalently specified by,

$$I_D(V_{GS}, V_{DS}; K, V_{ON}), \tag{5.4}$$

where three model parameters (actually, four if (W/L) is split into two parameters) are compressed into a single device parameter, $K= (W/L)C_G\mu$. Since our primary goal here is to explain TTFT device physics operation, we will usually avoid this type of model parameter compression since it tends to obscure the operating physics.

A non-ideal TTFT model, such as the discrete trap model summarized in Table 5.12, may also be specified in a functional form,

$$I_D(V_{GS},V_{DS}; (W/L), C_G, \mu, (m^*/m_o), N_{TRAP}, E_{TRAP}, n_{co}; T). \tag{5.5}$$

Note that this non-ideal model specification is more complicated, involving seven model parameters. Moreover, it also depends upon temperature, which is classified as a physical operation parameter, as distinguished from a model parameter. (Notice that independent variables, model parameters, and physical operating parameters are separated from one another by a semi-colon in functional form equations such as Eqs. 5.3-5.5).

Returning to Table 5.14, the second entry corresponds to a non-ideal model which may be represented in its functional form as,

$$I_D(V_{GS},V_{DS};(W/L),C_G,V_{ON},\mu(V_{GS}),S,R_S,R_D,R_{BULK},R_{SURFACE},R_d^{SAT}). \quad (5.6)$$

Explanation of the nature of the non-ideal model parameters included within this expression requires further explication of the remaining entries in Table 5.14, as briefly undertaken in the following.

- Trapping. Electron trapping in the channel or at the channel-insulator interface of an n-channel TTFT has already been considered in the context of the discrete trap model of Table 5.12 and the subthreshold augmentation procedure of Table 5.13. Physically, gate-voltage induced electrons in the channel may occupy conduction band states so that they can contribute to the drain current, but they may also be trapped. Thus, if Δn_c and Δn_t represent the injected concentrations of free and trapped electrons, respectively, the actual mobility, μ_{actual}, would be related to the drift mobility (no trapping), μ, by (Tickle 1969)

$$\mu_{actual} = \frac{\Delta n_c}{\Delta n_c + \Delta n_t}\mu . \quad (5.7)$$

  Since the first electrons induced into the channel are expected to be trapped, Eq. 5.7 shows that the actual channel mobility will be very small just beyond V_{ON}. However, as the gate voltage increases beyond V_{ON}, traps will fill so that a larger and larger fraction of the gate-bias-induced electrons are free to travel in the accumulation layer to the drain without being trapped. From a modeling perspective, the most complete way to account for trapping is to either calculate I_D directly using an appropriate non-ideal model or to assess $\mu(V_{GS})$, recognizing that variations in μ are a consequence of trap filling, as indicated in Eq. 5.7. A more convenient, but less precise way to handle trapping non-idealities is to assess the subthreshold swing, S. Trapping is the most important TTFT non-ideality.

- Interface roughness. As the gate voltage increases, electrons in the accumulation layer experience a larger transverse electric field, so that they are attracted closer to the channel-insulator interface where they experience more intensely scattering due to the roughness of the interface, resulting in a corresponding degradation in the channel mobility (Foty 1997; Taur and Ning 1998; Lundstrom 2000) with increasing V_{GS}. More interface roughness results in more mobility

degradation. For a TTFT, this gate voltage-induced reduction in the mobility may be modeled as (Foty 1997),

$$\mu(V_{GS}) = \frac{\mu_o}{1 + \theta(V_{GS} - V_{ON})}, \tag{5.8}$$

where μ_o is the low-field mobility and θ is a mobility degradation factor. This equation implies that the channel mobility will decrease with increasing V_{GS} once the second term in the denominator is nonneglibible compared to one. In our experience, interface roughness scattering is usually not very important except at exceedingly large gate voltages, for unoptimized TTFTs, or when the insulator is very rough (in the case of a bottom-gate configuration). Equation 5.8 is used in the simulation performed in conjunction with Fig. 5.11 in order to account for interface-roughness-induced mobility degradation associated with the use of a bottom-gate ATO insulator. Very often we have found that the rather large surface roughness of the ATO dielectric leads to a mobility overshoot in $\mu(V_{GS})$ curves, in which the increase in μ at low V_{GS}'s is ascribed to trap filling, whereas the decrease in μ at larger V_{GS}'s is attributed to interface roughness scattering (Chiang et al. 2005; Dehuff et al. 2005).

- Series resistance. If a poorly functioning contact to the channel layer exists at the source and/or at the drain, some of the applied source-drain voltage drops across this parastic resistance (Schroder 2006; Hong et al. 2007). This degrades the performance of a TTFT, resulting in a reduction in I_D and a distortion in the I_D-V_{DS} characteristics. Also, series resistance can lead to an *apparent* decrease in the channel mobility at high V_{GS}'s, i.e., the same trend observed when interface roughness is a dominant effect. Possible series resistance contributions include resistance between channel layer and source-drain contact materials, geometrical spreading resistance, and channel sheet charge resistance near the source or drain. The overall series resistance may be linear or nonlinear, in terms of the dependence of I_D on V_{DS}. Typically, series resistance is assumed to behave in a linear manner so that it can be modeled as a simple source and drain resistance, R_S and R_D. To date, we have found series resistance effects to be of negligible importance in determining the operation of a TTFT, at least for devices with large dimensions (Hung 2006).

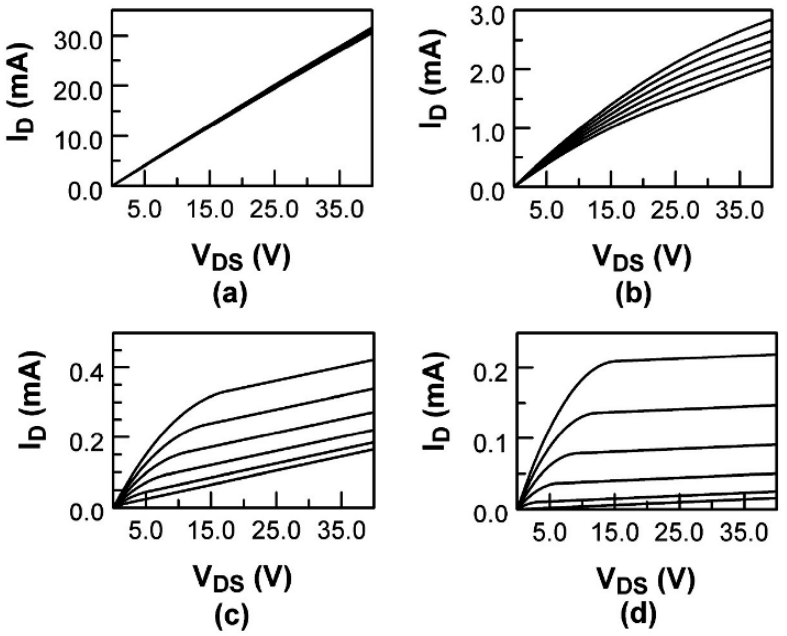

Fig. 5.15. Simulated TTFT I_D-V_{DS} curves for varying values of the equilibrium channel carrier concentration, using the 3-layer model. Plots (a)-(d) represent varying carrier concentrations of 10^{20}, 10^{19}, 10^{18}, 10^{17} cm^{-3} and result in V_{ON} ~ -230, -23, -2.3, -0.2 V, respectively. Model parameters used in this simulation: W/L = 5, $t_{channel}$ = 100 nm, C_G = 7 × 10^{-7} F/cm^2, μ = 0.5 cm^2/V-s, $R_{SURFACE} = 10^9 \Omega$. [from Hong et al. (2007)]

- Conductive channel. For proper TTFT operation, the channel layer needs to have a very low carrier concentration, i.e. < ~10^{16} cm^{-3}. Moreover, the channel layer back interface, i.e., the channel interface opposite to that formed with the gate insulator, should be depleted, not accumulated. If either of these conditions is not met, a low-resistance shunt path exists between the source and the drain. Figure 5.15 illustrates the types of problems encountered when one of these shunt resistances is too low. These simulations are generated using the 3-layer model (Hong et al. 2007), which assumes that accumulation layer current flow is shunted by a bulk channel or a back interface (surface) resistor, R_{BULK} and $R_{SURFACE}$, respectively, as is illustrated in Fig. 2.4. When the zero-bias channel layer electron concentration is extremely high, as shown in Fig. 5.15a, there is essentially no gate voltage control

of the channel conductivity so that the TTFT behaves as a resistor. As the channel carrier concentration is reduced, which is progressively indicated in Figs. 5.15b-d, the gate voltage control of the channel conductivity becomes more effective, although none of the I_D-V_{DS} curves shown can be completely turned off, nor do they exhibit hard saturation in which the slope of the I_D-V_{DS} curve is zero at large V_{DS}'s. Examples of `hard' and `soft' saturation are shown in Fig. 5.16. The degree of saturation can be quantified by assessing the channel resistance in saturation, which is defined as the inverse of the slope of an I_D-V_{DS} curve in the saturation regime of operation. For an ideal TTFT, $R_d^{SAT} = \infty$. A very simple way to account for a non-infinite channel resistance in a TTFT device model, such as those summarized in Table 5.11 and 5.12, is to multiply the pre-pinch-off drain current expression by $(1+\lambda V_{DS})$, where λ is equal to the reciprocal of R_d^{SAT} (Foty 1997). While the 3-layer model offers a very simple way to model a conductive channel, a much more detailed and precise way to account for conductive channel non-idealities is to use the comprehensive depletion-mode model (Hong et al. 2007). Hard saturation is a very desirable attribute, since many aspects of transparent electronics circuit design are facilitated if a TTFT exhibits hard saturation.

- Channel length modulation. At $V_{DS} = V_{DSAT}$, which defines pinch-off, the accumulation layer is no longer contiguous across the entire channel, as it is depleted near the drain. If V_{DS} is increased beyond pinch-off, the resulting drain-source overvoltage, i.e., V_{DS}-V_{DSAT}, depletes more of the channel, moving the depletion boundary away from the edge of the drain towards the source. Such a depletion of the channel decreases the effective channel length, L_{eff}, compared to the physical length of the channel, L. Since I_D is inversely proportional to the channel length, e.g., see Table 5.11, this reduction in the effective channel length leads to an increase in I_D. If the reduction in the channel length is non-negligible compared to the physical channel length, i.e., if the condition L_{eff}-L<<L is not satisfied, then a condition of hard saturation will not be achieved and $R_d^{SAT} < \infty$, as already discussed with respect Fig. 5.16. Channel length modulation can be accounted for in a TTFT device model in an identical manner as a conductive channel, i.e., by multiply the pre-pinch-off drain current expression by $(1+\lambda V_{DS})$, where λ is equal to the reciprocal of R_d^{SAT} (Foty 1997). Channel length modulation is anticipated to be most pronounced in TTFTs with small channel lengths.

For TTFTs with device dimensions exceeding 10 μm, we have not witnessed any evidence for this effect.

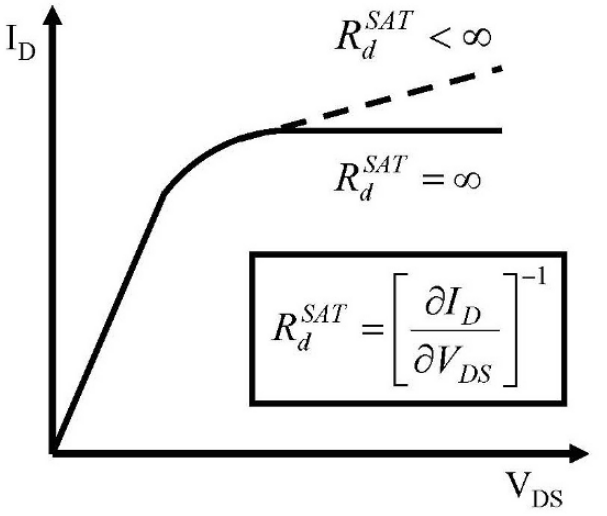

Fig. 5.16. I_D-V_{DS} curves illustrating `hard' saturation ( $R_d^{SAT} = \infty$ ) and `soft' saturation ($R_d^{SAT} < \infty$), where the channel resistance in saturation, R_d^{SAT}, as defined in the figure, is a quantitative indicator of the degree of saturation.

- Gate leakage / noise floor. As discussed previously in this section, V_{ON} is empirically established in a log(I_D)-V_{GS} transfer curve as being equal to V_{GS} where the I_D begins to increase above a baseline current due to the gate leakage and/or the instrumentation noise floor. In turn, knowing V_{ON} enables the minimum drain current to be assessed so that the drain current on-to-off ratio, I_D^{ON-OFF}, can be determined. When a log(I_D)-V_{GS} transfer curve is simulated, this minimum drain current is not known *a priori*, but must be independently assumed. Thus, the gate leakage / instrumentation noise floor constitutes a real-world non-ideality which helps to specify an important TTFT figure-of-merit, namely I_D^{ON-OFF}.

- Insulator leakage. Having appreciable gate insulator leakage is never a good thing. A larger gate leakage decreases I_D^{ON-OFF}, results in more TTFT power dissipation, and yields a TTFT which is more unstable and unreliable. Additionally, the channel mobility can be significantly overestimated in a TTFT with a leaky gate insulator since the estimated I_D is actually equal to $I_{DS} + I_{DG}$ instead of just I_{DS} and any overestimation of I_D will lead to a corresponding overestimation of the channel mobility. In our opinion, if the leakage current, I_G, in a TTFT is measured to be appreciable compared to I_D, nothing reliable can be inferred about the channel mobility of such a device. Thus, it is best to only perform a mobility assessment using a TTFT with neglibible gate leakage compared to I_D. The simplest way to account for gate leakage in a simulation is to model it using two resistors, R_{GS} and R_{GD}. However, the viability of such a simple model is questionable since charge storage within the insulator and non-linear injection and/or transport effects are ignored. Again, our bias is that the only reason for including gate leakage effects in a simulation is to ensure that it is so small that it can be ignored. There are already many unreliable channel mobility reports in the TTFT literature due to researchers not appreciating the crucial importance of reducing gate insulator leakage.
- Unpatterned channel, fringing current artifact. As mentioned in Section 2.2.2, perpherical current beyond the source-drain width, W, can flow in a TTFT with an unpatterned channel, as illustrated in Fig. 5.17. This extra fringing current leads to an overestimation of the channel mobility if I_D is assumed to be exclusively due to channel-width-confined drain current. If the channel mobility is found to increase with decreasing (W/L) in a TTFT with an unpatterned channel, this is a likely indicator of a fringing current artifact, although this trend has also been attributed to series resistance (Fortunato et al. 2004b & 2005). Although it is possible to attempt to analytically correct for this fringing current (Hong et al. 2007), the only reliable way to avoid this problem is to pattern the TTFT channel layer.

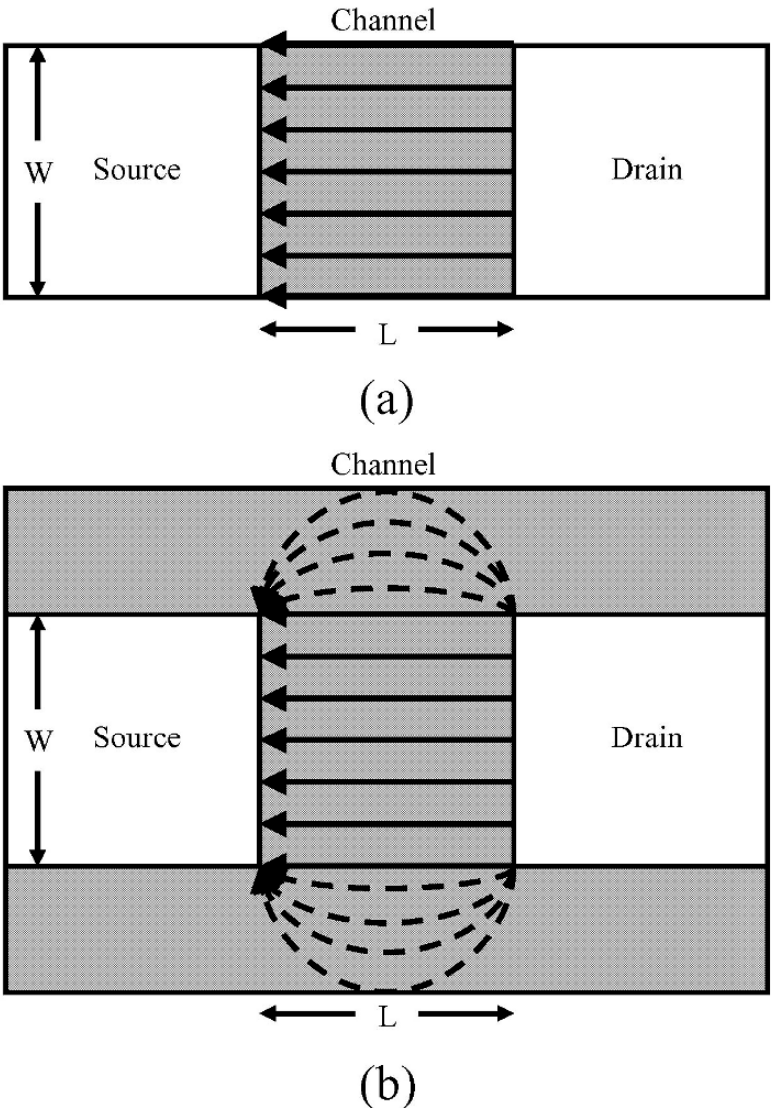

Fig. 5.17. Plan-view of current pathways in a transparent thin-film transistor (TTFT) with (a) a patterned and (b) an unpatterned channel layer. The existence of fringing current (dashed lines) leads to an overestimation of the channel-width-confined drain current (solid lines), and hence the channel mobility (after Hong et al. 2007).

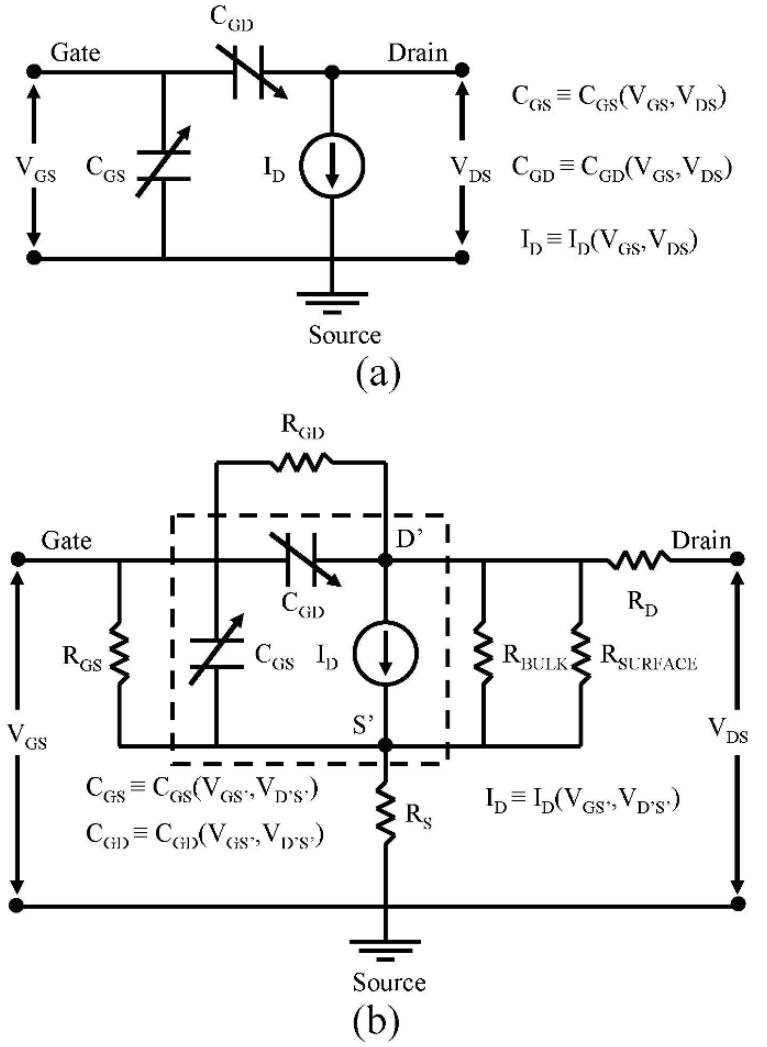

Fig. 5.18. Transparent thin-film transistor (TTFT) equivalent circuits for (a) an ideal device and (b) a non-ideal device. Possible non-ideal effects which could be accounted for in (b) include trapping (I_D), interface roughness (I_D), source & drain series resistance (R_S, R_D), a conductive channel (R_{BULK}), a conductive surface ($R_{SURFACE}$), channel length modulation (I_D), and insulator leakage (R_{GS}, R_{GD}).

Figure 5.18 displays two equivalent circuits which are useful for wrapping up and tying together this and the previous section on ideal and non-ideal TTFT behavior.

Figure 5.18a shows a TTFT equivalent circuit for an ideal device. The current source labeled I_D specifies a non-linear voltage-controlled-current-source, whose input-output functional dependence is specified by $I_D(V_{GS},V_{DS})$, and whose explicit device equations are those included in Table 5.11, which arise from square-law theory. Two capacitors are also included in Fig. 5.18a, C_{GS} and C_{GD}, connecting the gate-source and gate-drain, respectively. The arrow slashing through the symbolic capacitor parallel plates indicates that, in general, these are non-linear, voltage-controlled capacitors whose input-output functional dependence is specified by $C_{GS}(V_{GS},V_{DS})$ and $C_{GD}(V_{GS},V_{DS})$. For a static or DC TTFT model, these capacitors are open-circuited so that they do not explicitly appear in the equivalent circuit. Thus, inclusion of these capacitors implies development of a dynamic model.

The simplest way to model these capacitors is to assume that the total gate capacitance, C_{GATE}, is equal to the active capacitance of the channel under full accumulation so that,

$$C_{CHANNEL} = C_G \times W \times L\,, \tag{5.8}$$

where C_G is the gate capacitance density, plus the parasitic capacitance associated with lateral overlap, $L_{OVERLAP}$, of the source and drain electrodes with respect to the gate,

$$C_{OVERLAP} = C_G \times W \times L_{OVERLAP}\,, \tag{5.9}$$

and also to assume that the total gate capacitance is equally portioned between the source and the drain, so that

$$C_{GS} = C_{GD} = \frac{C_{GATE}}{2} = \frac{C_{CHANNEL} + C_{OVERLAP}}{2}\,. \tag{5.10}$$

This model implies that C_{GS} and C_{GD} are constant, linear or 'normal' capacitors, rather than the non-linear, voltage-controlled capacitors indicated by the symbols shown in Fig. 5.18a.

More accurate modeling of C_{GS} and C_{GD} would reveal that they are indeed non-linear, voltage-controlled capacitors and would also require that charge neutrality and capacitor non-reciprocity be satisfied. The interested reader is advised to consult the literature for further dynamic modeling treatments of MOSFETs and a-Si TFTs (Oh et al. 1980; Foty 1997; Kuo 2004a). Similar considerations should apply to the dynamic modeling of TTFTs.

Now turning our attention to Fig. 5.18b, first note that the ideal model equivalent circuit is contained within the dashed box shown in Fig. 5.18b. However, the I_D equations for this device would involve a non-ideal static or DC model, rather than the ideal, square-law model, and would account for effects such as trapping, interface roughness, and channel length modulation. Many of the non-idealities listed in Table 5.14 are explicitly accounted for in this non-ideal equivalent circuit, including series resistance (R_S, R_D), conductive channel effects (R_{BULK}, $R_{SURFACE}$), and gate insulator leakage (R_{GS}, R_{GD}). Note that if appreciable series resistance is present in a TTFT, the independent variables of the input-output functional form of I_D, C_{GS}, and C_{GD} for the non-ideal model now depend on voltages at internal nodes S' and D', rather than on externally applied voltages; e.g., $I_D(V_{GS},V_{DS}) \rightarrow I_D(V_{GS'},V_{D'S'})$. This is a consequence of the fact that some of the applied voltage is dropped across these parasitic resistances, R_S and R_D, so that not all of the applied voltage is available to induce charge into the accumulation channel and move it by drift down the channel.

5.4.3 Device stability

As transparent electronics technology matures, TTFT device stability becomes an increasingly important topic.

In this context, Fig. 5.19 provides an example of a typical stability trend that we have observed when an AOS channel layer is employed in a bottom-gate TFT fabricated using thermal SiO_2 grown on a heavily-doped silicon substrate. This SiO_2-Si bottom-gate substrate is convenient for rapid channel layer development, since thermal SiO_2 is an excellent gate dielectric in conjunction with an AOS channel layer. Also, such a structure is robust enough to sustain a high-temperature anneal, so that channel annealing trends can be established over a wide range of temperature. This SiO_2-Si substrate is used exclusively in the TFT stability studies reported in this section.

With regard to Fig. 5.19, device stability is assessed via constant-voltage bias-stress testing, which is accomplished by monitoring $\log(I_D)$-V_{GS} transfer curves as a function of time, at stress times of 0, 0^+, 10^3, 10^4, and 10^5 s. At each assessment time, three sets of electrical data are acquired: (i) a $\log(I_D)$-V_{GS} transfer curve at small V_{DS} (~1 V) for mobility extraction, (ii) a $\log(I_D)$-V_{GS} transfer curve at larger V_{DS} (~20–30 V) for I_D^{ON-OFF} extraction, and (iii) an I_D-V_{DS} output curve. Each transfer and output curve is swept in both forward and reverse directions for quantita-

tive evaluation of hysteresis, using a sweep rate of ~1 V/s. Each full set of stability data requires an acquisition time of ~4-5 minutes, thereby adding somewhat to the actual stress duration. Note that stress times of 0 and 0^+ refer to a procedure in which a full set of stability data is acquired twice in immediate succession, prior to when the constant-voltage stressing is initiated, so that early-stage aging can be evaluated.

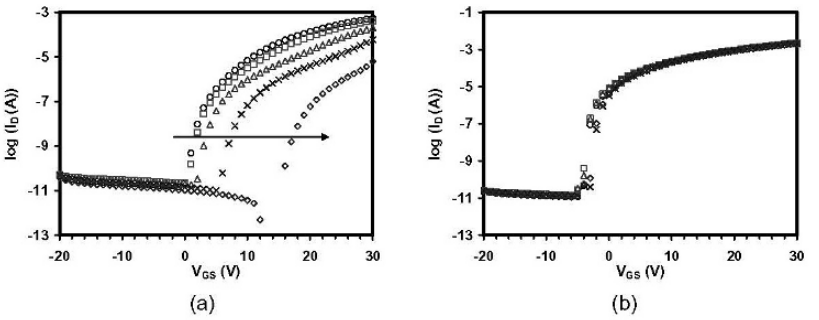

Fig. 5.19. Log(I_D)–V_{GS} transfer curve versus bias stress time plots for TFTs having a zinc indium oxide (ZIO) channel layer. ZIO channel layers are ~ 35 nm thick, deposited onto thermal SiO_2-Si bottom-gate substrates, and are prepared by rf magnetron sputtering followed by a post-deposition furnace anneal in air at either (a) 200 °C or (b) 400 °C. The arrow indicates the direction of increasing bias stress duration for stress times of 0 (circles), 0^+ (squares), 10^3 (triangles), 10^4 (x's), and 10^5 s (diamonds) [from (Hung 2006)].

The primary feature of Fig. 5.19 is that the device annealed at 200 °C is very unstable, while the 400 °C annealed device is quite stable, at least over the ~28 hour duration of the test conducted. This is a general trend which we have observed for several different types of AOS channel layer TFTs. Thus, we are very encouraged from these initial stability studies, and believe that AOS TTFTs are likely to be very stable, as long a channel layer can be annealed above a minimum temperature, which appears to be somewhat material-dependent, and a suitable, high-quality gate dielectric with properties approaching those of thermal SiO_2 is available.

Although more work is required to unambiguously establish a dominant instability mechanism for these AOS channel layer TFTs, several stability study-derived observations argue for identification of it as due to electron trapping near the channel-insulator interface, as discussed in the following paragraphs.

With respect to instability mechanism identification, we observe a decrease in the drain current measured in the saturation regime, i.e., I_{DSAT}, during a constant-voltage bias-stress measurement. According to the ideal, square-law model of Table 5.11,

$$I_{DSAT} \equiv \frac{W}{2L}\mu C_G\left(V_{GS} - V_{ON}\right)^2. \tag{5.11}$$

Since V_{GS} is held constant in a constant-voltage bias-stress measurement, a decrease in I_{DSAT} is ascribable to a decrease in μ or to an increase in V_{ON}. Our measurements invariably demonstrate that μ does not change appreciably, at least for a device which exhibits a respectable stability. Thus, the instability witnessed with respect to these AOS channel layer TFTs is associated with a positive shift in V_{ON}.

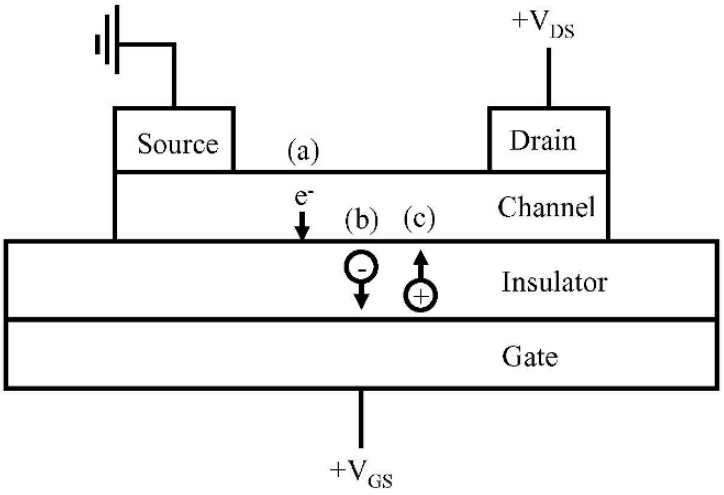

Fig. 5.20. Cross-sectional view of an n-channel TFT subjected to a positive gate bias. Three possible instability mechanisms are indicated, all of which would lead to time-dependent changes in V_{ON}. The instability mechanisms shown are (a) electron trapping at or near the channel/insulator interface, (b) negative mobile ion migration within the insulator towards the insulator/gate interface, and (c) positive mobile ion migration within the insulator towards the channel/insulator interface [after (Hung 2006)].

Figure 5.20 illustrates three types of charge migration - (a) electron trapping at or near the channel-insulator interface, (b) negative ion migration within the insulator towards the gate-insulator interface, and (c) positive ion migration within the insulator towards the channel-insulator interface - all of which could conceivably occur in an operating n-channel TFT,

and which would give rise to a V_{ON} shift. The direction of the shift in the turn-on voltage with aging, ΔV_{ON}, can be determined from

$$\Delta V_{ON} = \frac{-\Delta\gamma Q_{MIG}}{C_G}, \tag{5.12}$$

where C_G is the gate capacitance density, Q_{MIG} is the total charge density which migrates during aging, and $\Delta\gamma$ is the change in the charge centroid location of the migrating charge. Q_{MIG} is positive or negative, depending on the sign of the charge which migrates. $\Delta\gamma$ is positive if charge moves toward the channel-insulator interface and negative if it moves toward the gate-insulator interface. (The centroid can have a value between 0 and 1, i.e. $0 \leq \gamma \leq 1$. $\gamma = 0$ if all of the rearranged charge is located at the insulator/gate interface, and $\gamma = 1$ if all of the rearranged charge is located at the channel/insulator interface.) Thus, electron trapping at or near the channel-insulator interface yields a positive ΔV_{ON}, consistent with AOS TFT trends such as those shown in Fig. 5.19, whereas positive or negative ion migration in the insulator leads to a negative ΔV_{ON} shift. Although we have observed negative ΔV_{ON} shifts in bias-stress testing experiments, this is only observed when a poor-quality insulator is used such that ion migration appears to be the dominant instability mechanism (Hung 2007).

Further evidence for electron trapping at or near the channel-insulator interface as a likely instability mechanism is that $\log(I_D)$-V_{GS} hysteresis, when observed, is clockwise. As indicated in Fig. 5.21, clockwise $\log(I_D)$-V_{GS} hysteresis corresponds to a positive ΔV_{ON} shift. For reasons identical to those discussed previously in the context of Fig. 5.20 and Eq. 5.12, a positive ΔV_{ON} shift concomitant with clockwise hysteresis is consistent with electron trapping at or near the channel-insulator interface as an instability mechanism, and is not consistent with positive or negative ion drift in the insulator. Note that we do not always observe $\log(I_D)$-V_{GS} hysteresis in the electrical characteristics of our AOS channel layer TFTs. Moreover, when we do observe hysteresis, it is invariably most pronounced at a stress time of 0 s and, typically, is negligible for subsequent bias stress durations (Hung 2007).

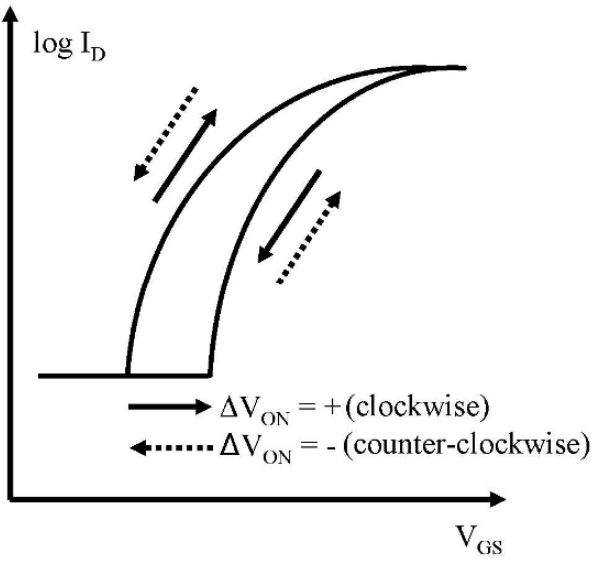

Fig. 5.21. Log(I_D)-V_{GS} transfer plot showing clockwise and counter-clockwise hysteresis. Clockwise hysteresis exhibits a positive shift in V_{ON} while counter-clockwise hysteresis results in a negative shift in V_{ON} [after (Hung 2006)].

Finally, we find that our instability is 'reversible' in the sense that if a previously tested TFT is retested after an extended period of rest time, typically we have retested after ~30 days, the retested log(I_D)-V_{GS} transfer curve is found to be virtually identical to that of the virgin device. This 'reversible' behavior is consistent with the instability mechanism of electron trapping at or near the channel-insulator interface, as an extended rest time allows sluggish deep traps the opportunity to re-emit, thereby resetting the TFT back into its initial state. If ion drift is the dominant instability mechanism, retesting after an extended period of rest time is expected to be 'irreversible' since there is no driving force for ions to diffuse back to their original location.

In summary, TFTs with AOS channel layers which are subjected to post-deposition anneals above ~400 ºC are found to exhibit excellent device stability when a high-quality gate insulator such as thermal SiO_2 is used. The TFT device instability, which is found to be more pronounced at lower channel annealing temperatures, appears to involve a mechanism in which electron trapping occurs at or near the channel-insulator interface. Evidence for this electron trapping instability mechanism includes: (i) a

positive V_{ON} shift, (ii) clockwise hysteresis in $\log(I_D)$-V_{GS} transfer curves, and (iii) aging reversibility after an extended period of rest time.

These encouraging stability results are of great potential interest for applications in which visible transparency is not necessarily a valued attribute. One particularly important possibility involves AOS channel layer TFTs replacing amorphous silicon (a-Si) TFTs for various types of large-area applications.

a-Si is an *inherently* an unstable or, more precisely, a metastable material (Powell et al. 1992; van Berkel 1992; Powell et al. 1993; Powell et al. 1996; Powell et al. 2002). In order for a-Si to be electrically useful, it must be hydrogenated. Oversimplifying the actual situation, the role of hydrogen in the amorphous network is to satisfy dangling bonds, so that related trapping states distributed across the band gap are, at least to a large extent, passivated. From a stability point-of-view, this is problematic since the distribution of states within the band gap is not stable but, it turns out, depends upon the Fermi level position, as established, for example, by an electrical bias in a TFT or by light excitation in a solar cell.

A conventional a-Si TFT employs a silicon nitride gate insulator and is subject to two types of instabilities - charge trapping and state creation (Powell 1992, van Berkel 1992). Charge trapping refers to the fact that silicon nitride is known to possess a large trap density such that electrons or holes injected into this insulator will be trapped, giving rise to a corresponding shift in the threshold voltage of the TFT. In passing, note that silicon dioxide does not exhibit appreciable charge trapping. The other relevant instability - state creation - is a process in which the distribution of states within the a-Si band gap is reshaped as a consequence of modulating the Fermi level. Fermi level modulation is accomplished, for example, at the interface of an a-Si TFT when a gate voltage is applied to create either an electron or hole accumulation at the interface. The interested reader is referred to the literature for a more detailed picture of the physics and chemistry of a-Si (Powell et al. 1992; van Berkel 1992; Powell et al. 1993; Powell et al. 1996; Powell et al. 2002).

What is the point of presenting this abbreviated a-Si background? Just this. The stability of commercial a-Si TFTs is based on ‘fixing’ the state creation instability in hydrogenated a-Si through the use of a poor-quality gate dielectric, silicon nitride, so that its carrier trapping instability can be used to counteract the state creation instability, which is inherent in a-Si because of its metastable nature. In other words, a new type of instability

is introduced to counteract the effects of an instability which cannot be eliminated.

When presented in this manner, this strategy might seem foolhardy. Nonetheless, it has been extraordinarily successful, primarily because the simple voltage switching application for which it is usually employed is relatively non-demanding so that this solution is quite adequate. Our contention, however, is that there are many emerging applications in which a-Si TFT technology is not an appropriate solution, given the inherent nature of its stability problem. We propose that oxide-based electronics, a major theme of this book although our focus is primarily directed at transparent applications, is a more appropriate technology for many of these types of applications. This theme is further developed in Chapter 6.

As a final note to conclude this section, we believe that organic field-effect transistor (OFET) technology faces the same challenges as a-Si TFT technology. OFET channel mobilities are often extremely low, typically significantly less than that of a-Si TFTs, having a theoretical upper limit of ~10 $cm^2V^{-1}s^{-1}$, with a highest reliably reported value of ~3 $cm^2V^{-1}s^{-1}$ (Dimitrakopoulos and Mascaro 2001). Moreover, we believe that the device stability of OFETs is inherently poor compared to oxide-based TTFTs. This stability trend arises primarily as a consequence of the strength of the bonding in these materials - the inclusion of weak, hydrogen-related bonds in organic materials versus strong, ionic-covalent bonds in inorganic oxides. From an electronics point-of-view, organic materials have two primary advantages - low-temperature processability and mechanical properties compatible with flexible substrates. If low-temperature deposited oxide-based TFT performance and stability can be improved, it is likely that oxide-based TFTs will be the active-electronics material set of choice for organic-inorganic nanolaminate structures which are likely to be the ultimate solution for low-temperature plastic substrate-based flexible electronics (we believe that organics will be useful in this regard, but more for their mechanical properties than their electronic functionality).

5.4.4 Alternative TTFT device types

Two alternative TTFT device types - double-gate and p-channel - are now briefly considered.

5.4.4.1 Double-gate TTFTs

A double-gate field-effect transistor is configured with both a top and a bottom gate. Although double-gate TFTs were demonstrated more than 25 years ago (Chen and Luo 1981a,b), double-gate MOSFETs are a topic of significant current interest (Taur 2001) since a double-gate configuration facilitates device scaling to ultra-small dimensions and provides more drain current. Ultra-deep submicron device scaling issues are not relevant to transparent electronics, but increasing the current drive is attractive, providing one impetus for considering the possibility of a double-gate TTFT. Another possible reason for pursuing the development of a double-gate TTFT is with respect to transparent charge-coupled device (CCD) applications, as discussed in Section 6.3.2.6. Although we have to date not fabricated a fully-transparent double-gate TTFT, we have constructed a double-gate TFT with a transparent zinc tin oxide channel, a SiO_2-silicon substrate bottom-gate, and a sputtered HfO_2 top gate. Basic operation of this double-gate TFT is illustrated in Fig. 5.22.

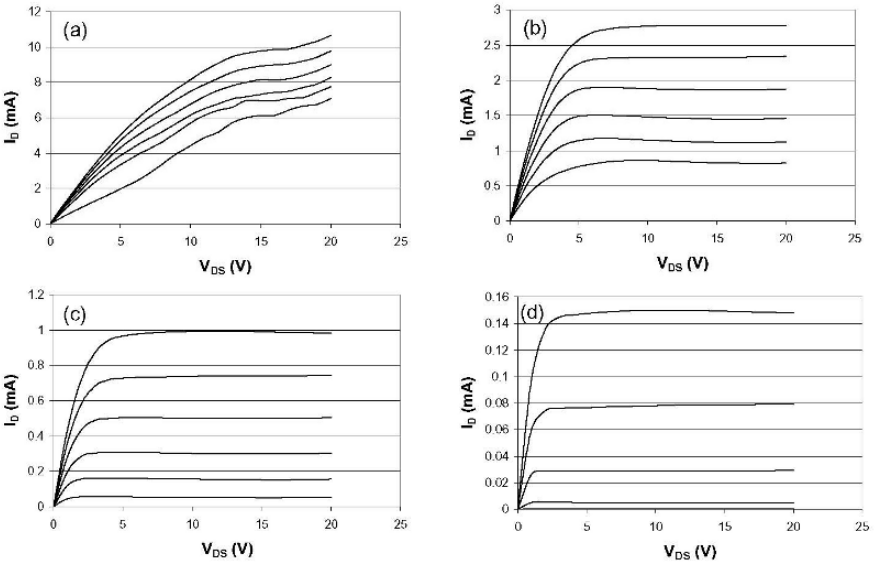

Fig. 5.22. I_D-V_{DS} characteristics for a double-gate TFT with a zinc tin oxide channel layer which is post-deposition annealed in air at 500 ºC. The 200 nm SiO_2-silicon substrate bottom gate is biased at 0, 10, 20, 30, and 40 V. The 160 nm HfO_2 top gate is biased as follows: (a) floating, (b) ground, (c) -2 V, and (d) -4 V. Gate leakage is ~ 10^{-10} A for the bottom gate and ~10^{-7} A for the top gate (Hong 2006).

5.4.4.2 p-channel TTFTs

In our experience, p-channel TTFTs are *much* more difficult to fabricate than n-channel TTFTs. The I_D-V_{DS} characteristics of our best result to date are given in Fig. 5.23. Although this device does indeed exhibit transistor behavior, its performance is very poor, having an exceedingly large turn-on voltage, $V_{ON} \approx$ -60 V and a very small incremental mobility, $\mu_{INC} \approx 0.01$ $cm^2V^{-1}s^{-1}$. Since V_{ON} is so large, the pinch-off condition is not achieved so that this device exhibits a `soft' saturation. Other undesirable attributes of this device include requiring an extremely high post-deposition annealing temperature of 800 °C and the fact that the channel layer is not completely transparent.

Why are p-channel TTFTs so much harder to realize compared to n-channel TTFTs? At least two factors appear to be significant.

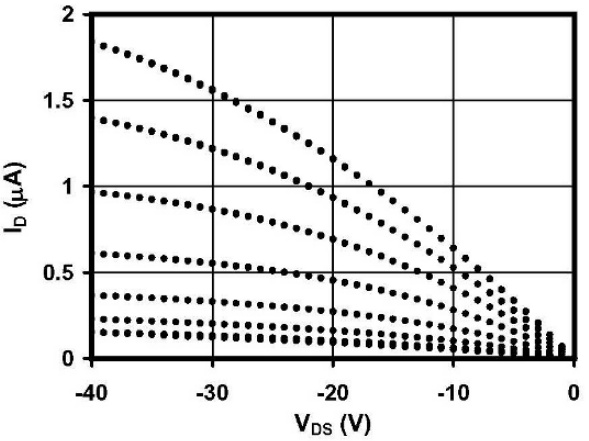

Fig. 5.23. I_D-V_{DS} curves for a p-channel TFT employing $CuZnO_x$ as the channel layer and a thermal SiO_2-silicon substrate bottom gate. The channel layer is subjected to a post-deposition furnace anneal in air at 800 °C in air. For this device, $V_{ON} \approx$ -60 V, $\mu_{INC} \approx 0.01$ $cm^2V^{-1}s^{-1}$, and W/L = 5 (Chiang 2006).

First, wide band gap materials which lean p-type, and hence are p-channel candidates, are not common and tend to usually contain either Cu or Ag. The d-band nature of the top of the valence band of Cu- or Ag-based materials will almost always result in a material with a very low hole mobility, as discussed in Section 4.4. Moreover, Cu- and Ag-based materials are usually difficult to process, which is partially a consequence of the high diffusivity of these monovalent cations.

A second reason why p-channel TTFTs are much more challenging to fabricate than n-channel TTFTs is that it is very difficult to make an Ohmic or injecting contact to a wide band gap p-type material unless it is heavily doped. To see that this is indeed the case, we can model the source-drain contact to the p-channel layer as a Schottky barrier, and then require that the Schottky barrier be near-zero or negative in magnitude, in order to ensure that it is Ohmic or injecting. From Table 5.5, this leads to the following constraint on the source-drain `metal' work function,

$$\Phi_M \geq \frac{IP_S - \Phi_{CNL}}{S} + \Phi_{CNL}, \tag{5.11}$$

where Φ_M = source-drain `metal' work function, IP_S = channel layer ionization potential, Φ_{CNL} = channel layer charge neutrality level, and S is the interface parameter. Consider the two limiting cases. In the no-screening limit S→1, so that $\Phi_M \geq IP_S$. In the perfect-screening limit S→0, so that $\Phi_{CNL} \geq IP_S$. The no-screening limit constraint is very difficult to meet, since IP_S is typically ~5.5-8 eV and we are aware of no metals or 'metal' contact materials with work functions this large. The perfect-screening limit constraint appears to be impossible to satisfy, since Φ_{CNL} will always be located within the band gap, usually within ~1 eV of the conduction band minimum for a wide band gap semiconductor (Wager 2007). Therefore, this assessment implies that it is very difficult, and probably impossible to form an Ohmic or injecting contact to a p-type channel layer which has a very low carrier concentration, as required for proper TTFT operation. Thus, unlike the case of an n-channel TTFT in which an injecting contact can be formed directly onto a low carrier concentration channel layer, formation of a low-resistance source-drain contact for a p-channel TTFT will require that the channel region under the contact be heavily doped in order to form a tunneling contact. This increases the process complexity of fabricating a p-channel TTFT compared to that of an n-channel TTFT.

Even though a p-channel TTFT appears at this time to be a very elusive goal, the availability of a complementary c-TTFT technology would be an exceedingly attractive outcome, given the numerous advantages of CMOS technology over NMOS technology, as discussed in Section 3.2. A final caveat must be considered. A viable c-TTFT technology would require that the p-channel hole mobility not be too much smaller than the n-channel electron mobility. Ideally, the electron and hole mobilities would be equal, and high. From a practical point-of-view, we believe that the p-channel hole mobility should be at least 1 $cm^2V^{-1}s^{-1}$ to hold promise for c-TTFT applications.

5.5 Alternative transistors

As addressed in Table 3.1, a current weakness of transparent electronics technology is its low-frequency performance. This severely limits its potential application space. Several types of alternative transistors are briefly considered in the following paragraphs - static-induction transistors (SITs), vertical TFTs, several types of hot electron transistors, and nanowire transistors - since they offer the potential for extending transparent electronics to higher operating frequencies. Versions of each of the specific alternative transistors discussed are shown in Fig. 5.24.

Transit time is a unifying concept for clarifying the appeal of all of the transistors sketched in Fig. 5.24. High frequency transistor operation is, to a large extent, established by the transit time, t_{TT}, which may be expressed as

$$t_{TT} = \frac{L}{v} \approx \frac{L}{\mu\xi} \approx \frac{L^2}{\mu V}, \tag{5.12}$$

where L = distance, v = velocity, μ = mobility, ξ = electric field, and V = voltage associated with of the transit of a carrier across a central base or channel layer within the transistor. The first approximate equality refers to the assumption that the electric field is sufficiently low to allow for the mobility to provide a good description of carrier transport as being linear with respect to ξ (Lundstrom 2000). The second approximate equality involves assuming a uniform electric field so that it is equal to the voltage applied across the layer divided by the thickness of the layer.

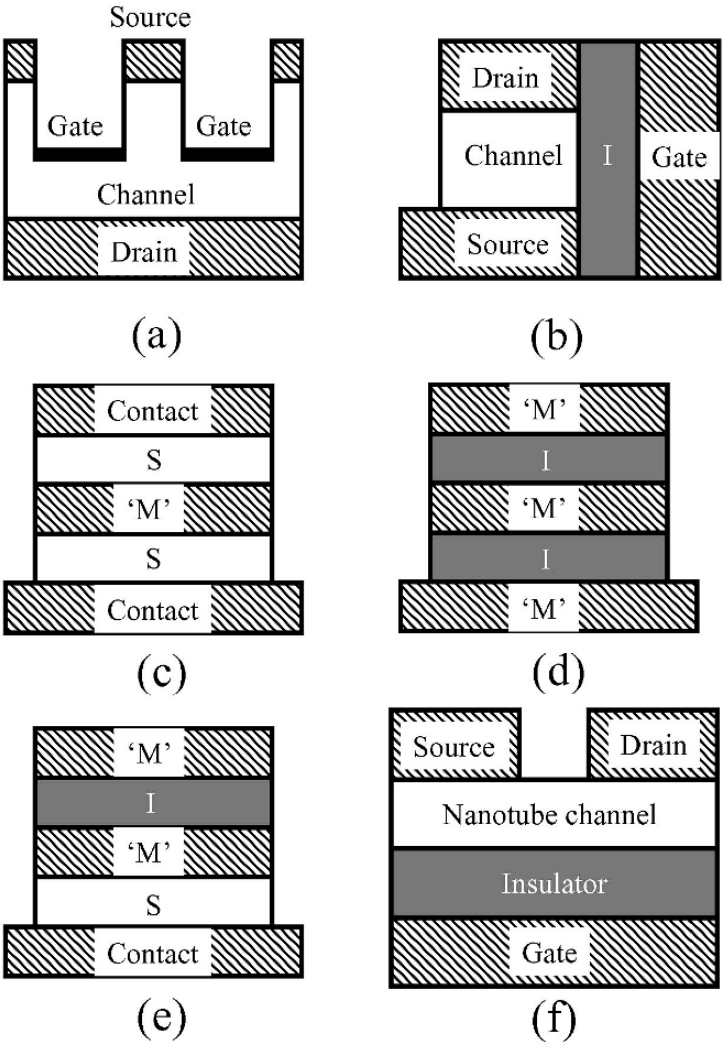

Fig. 5.24. Alternative transistor structures of potential use in transparent electronics for improving high-frequency performance. (a) static induction transistor (SIT), (b) vertical TTFT, (c) semiconductor-metal semiconductor (SMS), (d) 'metal'-insulator-'metal'-insulator-'metal' (MISIM), (e) 'metal'-insulator-'metal'-semiconductor (MISIM), and (f) nanowire transistor. (c), (d), and (e) are three different types of a hot electron transistor. The material indicated by cross-hatch is a transparent conductor, such as indium tin oxide (ITO). The SIT gate could be a Schottky barrier, a heterojunction, or a MIS capacitor.

Ignoring parasitic effects, the approximate maximum operating frequency of a transistor, f_T, is inversely proportional to its transit time,

$$f_T = \frac{1}{2\pi t_{TT}} \approx \frac{\mu V}{2\pi L^2}. \tag{5.13}$$

According to Eq. 5.13 there are three ways to increase the operating frequency of a transistor: (i) increase the applied voltage, (ii) increase the mobility, or (iii) decrease the transit distance. Solution (i) is undesirable since it leads to an increase in the power dissipated. Solution (ii), choosing a material with a very large mobility, is the primary motivation for the nanowire transistor given in Fig. 5.24f. Solution (iii), decreasing the transit length, is the strategy employed in all of the other transistors shown in Fig. 5.24, except for the nanowire transistor. The idea here is to shrink the transit length by building devices in which the transit is vertical rather than horizontal. It is much simpler and cheaper to make devices with very thin vertical dimensions compared to horizontal dimensions, which requires expensive lithography. Note that this transit length reduction solution is, to a certain extent, the most effective one, since the maximum operating frequency depends in an inverse quadratic manner on the transit length.

A few general aspects of the alternative transistors indicated in Fig. 5.24 are now briefly discussed. The interested reader is referred to the literature cited below for a more in-depth treatment of each type of device.

One possible realization of a transparent static-induction transistor (SIT) is given in Fig. 5.24a (Oxner 1982; Pozela 1993; Nishizawa et al. 2002; Ng 2002; Sze and Ng 2007). The material indicated by cross-hatch is a transparent conductor, such as indium tin oxide (ITO), and all of the other layers could, in principle, also be transparent. The essential feature of this device is that carriers are injected from the source and transit vertically to the drain where they are collected. The intent of the gate is to provide some degree of electronic modulation of this source-drain current. The gate could consist of a Schottky barrier, a heterojunction, or a MIS capacitor. In practice, it is difficult to obtain the desired degree of gate control since lateral electric field control is required. An SIT has non-saturating current-voltage characteristics, similar to a vacuum triode, rather than the more desirable saturating characteristics obtained with a FET or a TFT. SITs have recently been explored as a means of improving the high-frequency performance of organic transistors (Kudo et al. 1998; Wang et al. 1999; Zorba and Gao 2005; Watanabe and Kudo 2005).

The vertical TTFT shown in Fig. 5.24b is a TTFT analog of the a-Si vertical TFT proposed in 1984 (Uchida et al. 1984). Again, the key feature of this device is vertical transport of carriers from the source to the drain. An important challenge for the realization of this type of device is side-wall deposition to obtain a high-quality, pinhole-free gate insulator. This would probably be most readily accomplished using atomic layer deposition.

Three types of transparent hot electron transistors - semiconductor-metal semiconductor (SMS), 'metal'-insulator-'metal'-insulator-'metal' (MISIM), and 'metal'-insulator-'metal'-semiconductor (MISIM) - are sketched in Figs. 5.24c-e (Moll 1963; Luryi 1990; Pozela 1993; Ng 2002; Reuss et al. 2006; Sze and Ng 2007). The hot electron transistor is a very old device concept. The basic idea is to launch heated carriers from an 'emitter' across a very thin 'base' layer, and to hopefully extract some of them in the 'collector'. The emitter-base and collector-base biases are used to control injection and extraction, respectively. As evident from the electrode nomenclature employed, hot electron transistor operation is similar to that of a bipolar junction transistor. Different materials combinations may be used to achieve hot electron injection, transit, and extraction, thereby yielding different types of hot electron transistor. Typically, hot electron transistors have poor base transport factors, rendering their overall electrical performance poor. If this issue can be suitably addressed in the context of transparent electronics via, for example, compositional grading and ensuring that the base is exceedingly thin, hot electron transistors may be able to significantly extend the range of operating frequency.

A final example of an alternative type of transistor which could potentially improve the high-frequency performance of transparent electronics in a dramatic fashion is a transparent nanowire transistor, an example of which is indicated in Fig. 5.24f. Note that this topology is identical to that of a bottom-gate TTFT, except that the channel is no longer a thin-film layer but, rather, is either a nanowire or a nanowire bundle. ZnO nanowire transistors with spectacular channel mobilities of ~1200-4120 $cm^2V^{-1}s^{-1}$ have been reported (Chang et al. 2006). Although this device was not completely transparent, since ZnO, SnO_2 (Zhang et al. 2004), and In_2O_3 (Liu et al. 2005) nanowires and/or nanowire transistors have been reported, it seems likely that a transparent nanowire transistor is not far off.

6 Transparent Circuits

6.1 Introduction

Very little work has been reported to date related to transparent circuits, and has been limited to inverters and ring oscillators (Presley et al. 2006; Kumomi et al. 2006). Thus, the first topic discussed in this chapter relates to the process flow and performance of these transparent circuits. The remainder of this chapter of necessity has a more speculative flavor, since devices, circuits, and applications are discussed which have not yet been reduced to practice.

6.2 Exemplary transparent circuit process flow

The process flow employed in the realization of transparent inverters and ring oscillators is overviewed (Presley et al. 2006) in order to provide a case-study glimpse of materials/device/process-integration/circuit considerations of relevance in the realization of a transparent circuit.

6.2.1 Transparent ring oscillator process flow

Transparent circuits are fabricated using a staggered, bottom-gate TFT configuration; the fabrication process includes eight primary steps and employs four masks defining the (i) gate electrode, (ii) gate insulator vias, (iii) the channel, and (iv) source and drain traces. Figure 6.1 gives an overview of the process flow for the fabrication of a transparent ring oscillator; a detailed discussion follows.

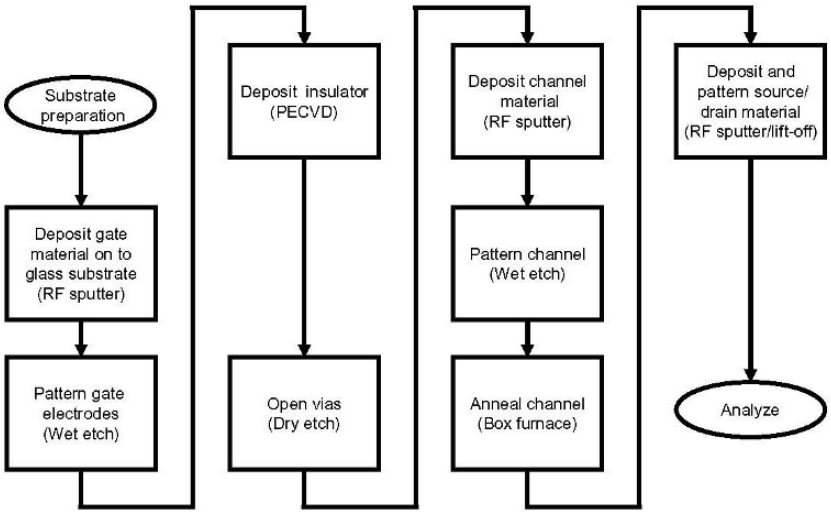

Fig. 6.1. Overview of the process flow for the fabrication of a transparent ring oscillator.

Fabrication of the transparent circuit begins with a Corning 1737 glass substrate, coated with ~200 nm rf sputtered indium tin oxide. Corning 1737 is chosen as the substrate for several reasons, including its relatively smooth surface and high processing temperature compatibility. Corning 1737 has a typical surface roughness of <0.02 μm peak-to-peak over a 5 mm sample distance, which makes it a suitable substrate. Another favorable property of Corning 1737 is its high softening point of ~975 ˚C. ITO is chosen as a gate contact due to its high optical transparency and good conductivity, as discussed in Chapter 1. Additionally, ITO provides high wet etch selectivity between the gate and channel layer (which is deposited in a later step). ITO gate electrodes are defined using standard photolithographic patterning and a hydrochloric acid (HCl) wet etch.

Even though all of the constituent layers in the transparent circuit are highly transparent, no special procedure is required for manual optical mask alignment since thin film edges are visible under optical microscope inspection. However, automated alignment of highly transparent layers may prove to be problematic. One route to circumvent this potential problem is to use nontransparent alignment marks for all subsequent masking steps.

Returning to Fig. 6.1, after patterning the gate electrode, the insulator is deposited. Silicon dioxide is used as the gate dielectric for process integration compatibility and based on our deposition capabilities. The silicon dioxide layer (~100 nm) is deposited via plasma-enhanced chemical vapor deposition (PECVD) using SiH_4 diluted with He and N_2O as precursor gases. Contact to gate electrodes is established through vias opened using reactive ion etching of the silicon dioxide.

The next step in the fabrication of transparent ring oscillators is deposition of the channel material. Selection of an appropriate transparent semiconductor to be used as a channel layer requires assessment of available materials and their properties. Important properties include the turn-on voltage, the carrier mobility, and ease of material patterning. Table 6.1 gives typical material properties for previously investigated transparent semiconductors, which could be utilized in transparent circuits.

Table 6.1. Selected material properties (as established at OSU) of transparent semiconductors which have been investigated as channel materials for TTFTs.

Channel material properties	Zinc indium oxide (ZIO)	Zinc tin oxide (ZTO)	Zinc oxide (ZnO)	Indium gallium oxide (IGO)	Indium gallium zinc oxide (IGZO)
Turn-on voltage (V)	-10	-2	-5	2	0
Mobility ($cm^2V^{-1}s^{-1}$)	40	25	5	15	10
Wet etchability	High	Low	High	High	High

The channel mobility is of particular importance in the context of material selection, since it strongly affects the maximum operating frequency of a circuit. From Table 6.1, zinc indium oxide (ZIO) clearly has the highest mobility of all of the materials considered (Dehuff et al. 2005). However, considerations other than mobility sometimes determine which material is actually selected for a particular circuit implementation.

For example, the fabrication of inverter-based ring oscillators without the use of level-shifting circuitry (as discussed in Section 6.3.2) requires that the turn-on voltage, V_{ON}, be near zero. Examining the material properties presented in Table 6.1, it is apparent that several transparent semiconductors have turn-on voltages that are suitable for the fabrication of ring oscillators, including zinc tin oxide (ZTO), zinc oxide (ZnO), indium gallium oxide (IGO), and indium gallium zinc oxide (IGZO) (Hosono et al.

2004; Chiang et al. 2005; Chiang et al. 2007). However, even though ZIO has the highest mobility, it is not a good candidate due to its strongly negative turn-on voltage.

Device integration also requires consideration of a material's etchability and etch selectivity with respect to neighboring layers. Possible material choices are further restricted if a high degree of wet etchability is required. As a result of this consideration, either ZnO, IGO, or IGZO are considered to be suitable candidates for transparent ring oscillator applications.

Using this channel layer material selection methodology, IGO was chosen as the transparent semiconductor employed in the fabrication of transparent ring oscillators (Presley et al. 2006). The IGO channel layer (40-50 nm) is deposited by rf magnetron sputtering from a ceramic target (Cerac, Inc.; 1:1 molar ratio of In_2O_3:Ga_2O_3). The channel is patterned using a diluted HCl wet etch and the sample is subsequently subjected to a 500 ˚C furnace anneal for one hour. The furnace anneal is thought to promote local atomic rearrangement, and thereby reduce the trap density present in the semiconductor, resulting in an increased mobility. In addition, the furnace anneal improves device (bias stress) stability.

To complete fabrication of the transparent ring oscillators, the source and drain contacts are deposited and patterned. ITO is chosen as the source-drain contact material for reasons identical to those given for its use as a gate contact, specifically high transparency and high conductivity. The ITO source-drain contacts (150-200 nm) are deposited by rf magnetron sputtering from a ceramic target (Cerac, Inc.; In_2O_3:Sn 10% wt.). Patterning is accomplished through the use of lift-off, rather than wet etching, due to poor etch selectivity between the ITO and the IGO layers.

Finally, it should be noted that another group has recently fabricated inverters and ring oscillators utilizing IGZO as the transparent semiconductor, sputtered silicon dioxide as the gate dielectric, and glass as the substrate (Kumomi et al. 2006). Although opaque electrodes (titanium and gold) are used in this circuit, the process could be easily modified to yield a fully transparent circuit.

6.2.2 Other considerations

The ring oscillator process flow previously presented does not require an interlayer dielectric because the source-drain layer and the gate electrode

layer are used as interconnects. As circuits become more complex, additional interconnect levels and interlevel dielectric/passivation layers will be necessary. Integrated circuit passivation is critical for mechanical/chemical protection and for subsequent integration with other components in a system. While TTFT passivation has not been extensively investigated, results presented to date suggest that successful passivation is somewhat material- and process-dependent. Nomura et al. successfully fabricated a top-gate IGZO TTFT using Y_2O_3 as a gate dielectric (which essentially represents a self-passivated channel, although with a relatively high dielectric constant, which is non-optimal for interlevel dielectric applications) (Nomura et al. 2004b).

As previously discussed in Section 2.2.3, passivation of a TTFT channel layer surface can be tricky (Hong and Wager 2005). Our experience to date suggests that many TTFT channel layer surfaces behave in a manner similar to that of a ZnO surface (Mark 1965; Many 1974; Eger et al. 1975), as illustrated in Fig. 6.2 and described as follows.

The adsorption of oxygen onto an n-type ZnO surface can be described in the context of acceptor-like surface state behavior (Mark 1965; Many 1974; Eger et al. 1975). As indicated in Fig. 6.2a, when molecular oxygen is physisorbed (weakly bonded) onto a ZnO surface, it is electrically neutral. However, if an electron from the ZnO conduction band is captured by the physisorbed molecular oxygen (dashed arrows of Fig. 6.2a), this electronic charge transfer process results in the formation of strong bonding (chemisorption) of the oxygen to the surface. This electron trapping process results in a depletion or loss of conduction band electrons from the ZnO surface. Concomitantly, the chemisorbed oxygen is now negatively charged. Thus, physisorbed and chemisorbed surface oxygen constitute the empty and filled states, respectively, of an acceptor-like surface state. The critical thing to note in the context of TTFT operation is that chemisorption of oxygen on an air-exposed surface tends to deplete the ZnO surface, thereby providing natural passivation of the surface.

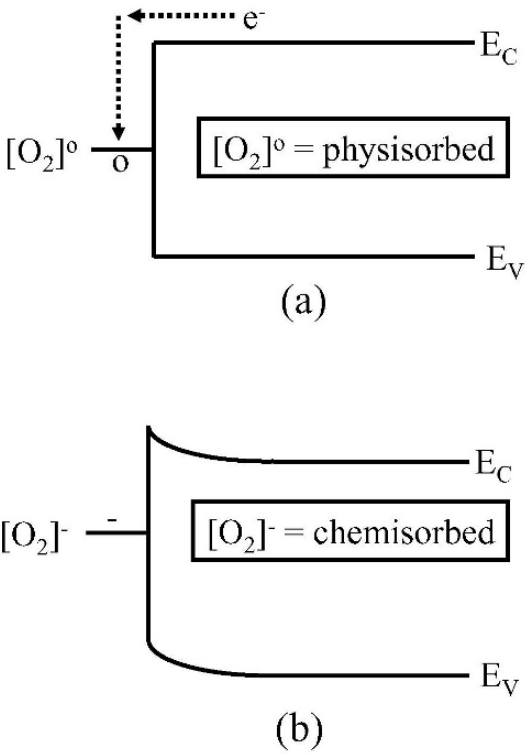

Fig. 6.2. Air-exposed channel layer depletion mechanism. (a) Energy band diagram at flat-band, illustrating that surface physisorbed molecular oxygen is electrically neutral. If an electron from the conduction band is trapped (dashed arrows), then (b) molecular oxygen becomes negatively charged and is chemisorbed to the surface. Conduction band electron trapping by molecular oxygen results in a depletion of the surface, as evident from the upward band-bending illustrated in (b). Note that the electronic energy state associated with the surface-adsorbed molecular oxygen is acceptor-like, since it is neutral when empty (no electron trapping) and negatively charged when filled (after electron trapping).

When another layer is subsequently placed upon an air-exposed ZnO surface, the resulting interface is not necessarily terminated in a self-passivating manner. Typically, an insulator would be placed upon a channel layer surface in order to accomplish passivation.

If we model this passivation insulator-channel layer interface as a heterojunction, as discussed in Section 5.2.3, Table 5.8 indicates that proper passivation would require that the conduction band discontinuity, ΔE_C, be

positive (assuming that material 1 is the channel layer and material 2 is the insulator) and ideally as large as possible. In turn, according to Table 5.8, this is most readily achieved when the channel layer electron affinity is larger than that of the insulator (i.e., $\chi_{CHANNEL} > \chi_{INSULATOR}$; the larger the difference in electron affinity, the better) and that the insulator layer charge neutrality level is greater than or equal to that of the channel layer [i.e., $\Phi_{CNL}(\text{insulator}) \geq \Phi_{CNL}(\text{channel})$]. Physically, this latter constraint ensures that interface state charge transfer either does not occur [i.e., when $\Phi_{CNL}(\text{channel}) = \Phi_{CNL}(\text{insulator})$], or that it occurs in such a manner that the channel layer is left depleted, rather than accumulated.

Alternatively, we could model this passivation insulator-channel layer interface as an insulator-semiconductor (IS) interface, which is similar to the MIS capacitor interface considered in Section 5.2.4. From this perspective, the fifth equation included in Table 5.10 for the flatband voltage, V_{FB}, is applicable if the metal-semiconductor work function difference term, ϕ_{MS}, is ignored. For proper channel layer passivation, a positive V_{FB} is desired. Thus, the IS interface V_{FB} equation indicates that positive charge in the passivation insulator, at the interface, or in the channel layer is undesirable. Note that if stable negative charge exists in a passivation insulator, this would be advantageous for accomplishing channel layer passivation.

Summarizing the last few paragraphs, our picture of channel layer passivation is as follows. An air-exposed surface is naturally passivated because of the acceptor-like nature of oxygen surface adsorption. If an insulator is deposited onto the channel layer surface, the resulting surface/interface is terminated in a different manner. For proper channel layer passivation, it is desirable that $\chi_{CHANNEL} > \chi_{INSULATOR}$, $\Phi_{CNL}(\text{insulator}) \geq \Phi_{CNL}(\text{channel})$, and that either no charge or stable negative charge exist within the passivation insulator.

If a channel layer is improperly passivated, an electron accumulation layer exists at the passivation insulator-channel layer interface. This accumulation layer constitutes an electrical shunt path at this interface, as illustrated in Fig. 2.4, which can greatly degrade TTFT performance, as shown in Figs. 2.3 and 5.14. A processing methodology leading to effective passivation of a ZTO surface is briefly overviewed in Section 2.2.3 (Hong and Wager 2005). More passivation work is required before transparent electronics can be considered to have reached a mature stage of commercialization.

One final topic - top- and bottom-gate TTFT structures - merits a brief comment, and serves as a conclusion to this section. Multiple device configurations may be employed when fabricating a TTFT, including top- or bottom-gate designs. Determining which design to implement is generally an application-specific undertaking. In certain situations a top-gate design may be required for process compatibility, e.g., a transparent channel layer which requires a post-deposition anneal at a high temperature which is incompatible with that of the dielectric. A top-gate design could potentially have the added benefit of yielding a higher channel mobility, if the surface of the channel layer is smoother than that of a bottom-gate dielectric. A smoother transparent channel layer-gate insulator interface reduces interface roughness scattering, which improves the channel mobility (Kumomi et al. 2006). A bottom-gate design could be required in other situations. For example, if a gate dielectric is deposited using solution processing, some solvents could negatively affect the transparent channel layer performance. In such a case, a bottom-gate design would be beneficial. Finally, double-gate designs may be required for certain high-performance or non-TTFT oriented applications, such as presented in Section 6.3.6

6.3 Exemplary transparent circuits

The only transparent circuits reported to date - transparent inverters and ring oscillators (Presley et al. 2006; Kumomi et al. 2006) - are reviewed first in this section, with emphasis on the work performed at OSU, since few other details related to transparent circuits are yet available in the literature. The remainder of this section is devoted to a discussion of other examples of transparent circuits and transparent circuit applications. This treatment is inherently somewhat speculative since these circuits and applications have not yet been reduced to practice.

6.3.1 Transparent inverters and ring oscillators

As discussed in Section 6.2 in the context of process flow and integration, transparent inverters and ring oscillators have been fabricated using IGO as the transparent semiconductor (Presley et al. 2006).

The transfer characteristic for a transparent inverter is shown in Fig. 6.3. The inverters consist of two n-type IGO TTFTs: a control transistor and a load transistor. In Fig. 6.3, the gate of the load transistor (V_{load}) and drain

voltage (V_{DD}) are biased to 30 V. The width and length of the control transistor are 2400 μm and 60 μm, respectively; the width and length of the load transistor are 600 μm and 60 μm, respectively.

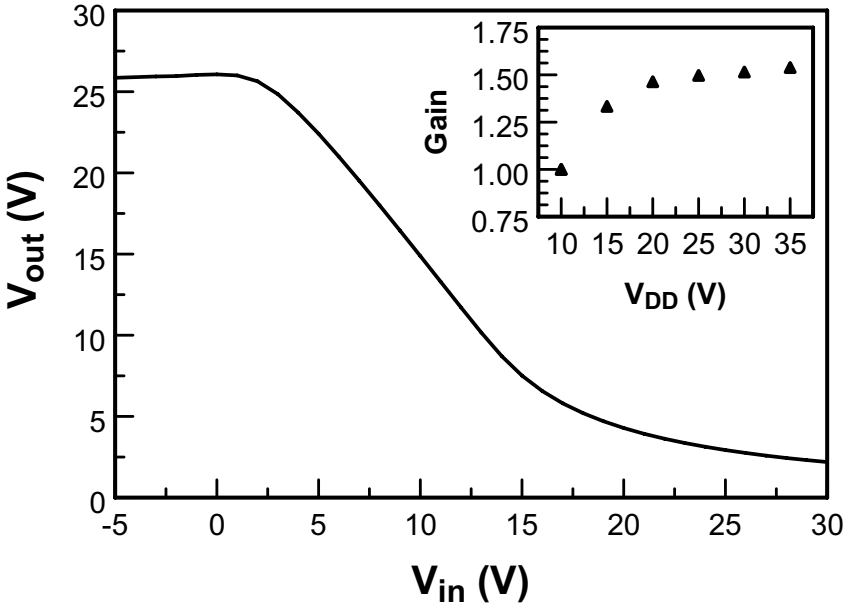

Fig. 6.3. Transfer curve for a transparent inverter fabricated using IGO-based TFTs and with V_{DD} and V_{load} = 30 V. The inset shows inverter gain as a function of V_{DD}. Reprinted from Solid State Electronics, 50, Presley R E, Hong D, Chiang H Q, Hung C M, Hoffman R L, Wager J F, Transparent ring oscillator based on indium gallium oxide thin-film transistors., 500-503, Copyright 2006, with permission from Elsevier.

The inverter shown in Fig. 6.3 exhibits the requisite characteristics needed to fabricate a ring oscillator using n-type transistors, without the use of level-shifting circuitry, as elucidated in the following discussion. First, notice that the switching voltage (the input voltage at which the output voltage begins to decrease) occurs at a positive V_{in} value; this ensures that the control transistor can be shut off during ring oscillator operation and corresponds to a near-zero voltage for the control transistor. Additionally, the peak gain (dV_{out}/dV_{in}) is ~1.5 for the transfer curve shown in Fig. 6.3; a gain greater than 1 is required for signal propagation (i.e., switching of the next inverter). The gain is affected by the ratio between drive and load TFT impedance and is thus affected by the channel mobility, device geometry, and biasing conditions. The inset of Fig. 6.3 shows the inverter gain as a function of V_{DD} (with $V_{load} = V_{DD}$) for an IGO-based

inverter; as V_{DD} is increased from 10 to 35 V, the inverter gain increases with increasing V_{DD}.

The oscillation frequency as a function V_{DD} for a five-stage transparent ring oscillator is shown in Fig. 6.4 (in all cases, V_{load} is equivalent to V_{DD}). As expected, the oscillation frequency increases as V_{DD} is increased; the maximum frequency of oscillation is ~9.5 kHz. A linear trendline is overlaid on the data, showing a fairly linear dependence of the oscillation frequency with increasing V_{DD}; the deviation from linearity at low-V_{DD} is a consequence of the non-ideal V_{GS} dependence observed in the channel mobility, as discussed in Section 5.3.2.

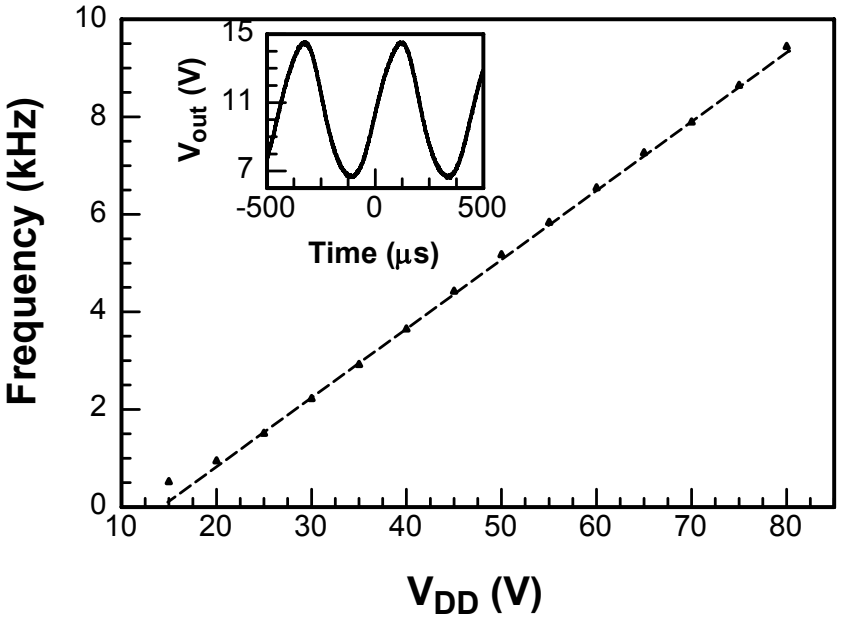

Fig. 6.4. Oscillation frequency as a function of V_{DD} for a five-stage ring oscillator fabricated using IGO-based TTFTs. The inset shows the output characteristic when V_{DD} is 30 V. Reprinted from Solid State Electronics, 50, Presley R E, Hong D, Chiang H Q, Hung C M, Hoffman R L, Wager J F, Transparent ring oscillator based on indium gallium oxide thin-film transistors., 500-503, Copyright 2006, with permission from Elsevier.

The inset of Fig. 6.4 shows the output characteristic of a five-stage transparent ring oscillator. Measurements are obtained through an output inverter stage which is used for non-intrusive electrical probing, with V_{load}

and V_{DD} = 30 V. The DC offset voltage is ~10 V and the peak-to-peak voltage and frequency of oscillation are ~8 V and ~2.2 kHz, respectively.

6.3.2 Full-wave rectifier

Alternating-current (AC) to direct-current (DC) conversion is often accomplished using a full-wave rectifier. Figure 6.5(a) shows a conventional full-wave rectifier realized using pn-junctions as the diode elements responsible for rectification. As discussed in Section 5.3.1, transparent pn junctions are not readily available in the context of transparent electronics. However, a transparent full-wave rectifier can still be fabricated, as illustrated in Fig. 6.5(b), using diode-tied n-TTFTs in which the gate and drain of each TTFT are connected together. Note that the rectifier illustrated in Fig. 6.5(a) is capable of operating at higher frequencies than that of the transparent rectifier depicted in Fig. 6.5(b), due to the additional parasitic overlap capacitance of a TTFT. However, transparent full-wave rectifiers will most likely be initially employed in low-frequency applications, so that this liability is not expected to be critical.

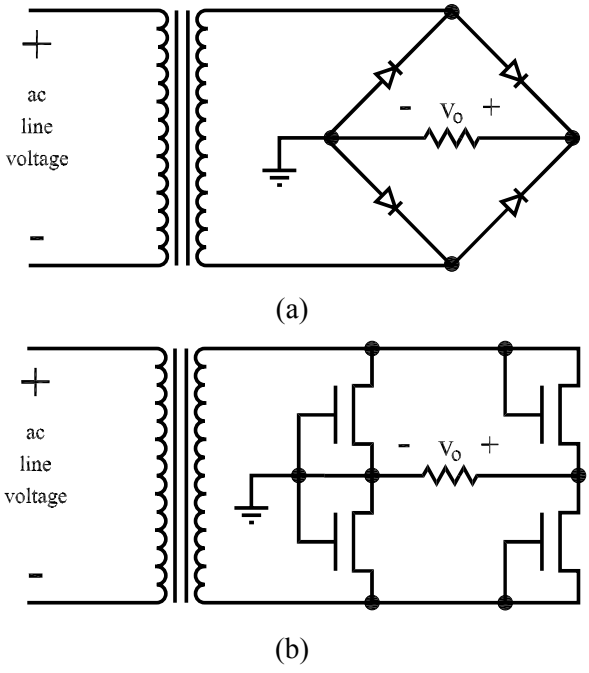

Fig 6.5. Full-wave rectifiers for AC to DC conversion. (a) a conventional pn-junction rectifier, and (b) a transparent rectifier using diode-tied, n-TTFTs.

6.3.3 Level-shifting circuits

As discussed in Chapter 2 and Section 5.3, some TTFTs operate in depletion-mode rather than in the more advantageous enhancement-mode. If such a TTFT is driven by an upstream circuit that only operates between zero and some positive voltage, then this depletion-mode TTFT could never be turn-off and, therefore, would be incompatible with the upstream circuit. If possible, the best option is usually to choose a TTFT which is enhancement-mode, and thus has a positive turn-on voltage (for an n-TTFT). If enhancement-mode TTFTs are unavailable, or if one desires to use a depletion-mode TTFT (to obtain a larger current drive, for example) a level-shifting circuit, such as the one shown in Fig. 6.6, may be required. In a level-shifting circuit, the input voltage is shifted so that it is within the desired range of the output circuit. The level-shifting circuit shown in Fig. 6.6 utilizes a two-transistor stack as a voltage-divider to shift the input voltage into the desired range. However, the addition of a level-shifting circuit decreases the operating frequency and increases level of the circuit complexity.

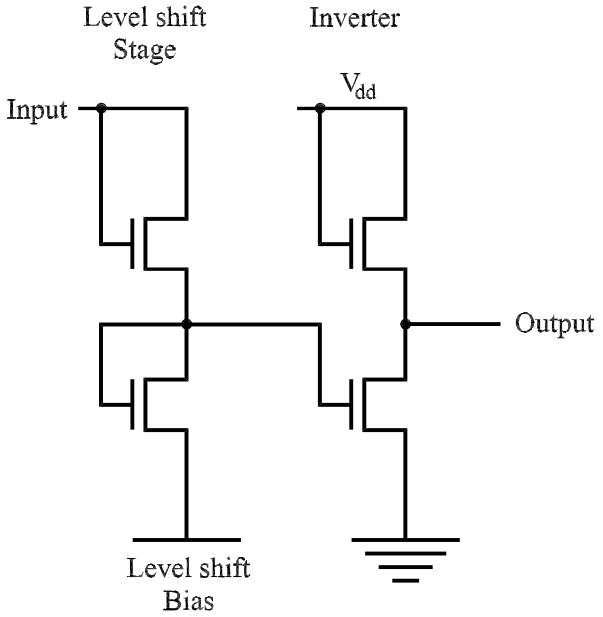

Fig. 6.6. A level-shifting circuit integrated onto the input of an inverter. This level-shifter uses a voltage-divider to shift the input voltage.

6.3.4 AMLCD transparent switch

Today, active-matrix liquid-crystal displays (AMLCDs) are ubiquitous. They are used extensively in small displays (e.g., digital cameras, camcorders, personal digital assistants (PDAs), cell phones, etc.) and medium sized displays (e.g., laptop computers, desktop computer monitors, etc.), and are becoming more common in the large display market (e.g., televisions, home theaters, etc.). AMLCDs currently constitute an ~$40B market, which is estimated to reach ~$100B by 2010 (den Boer 2005).

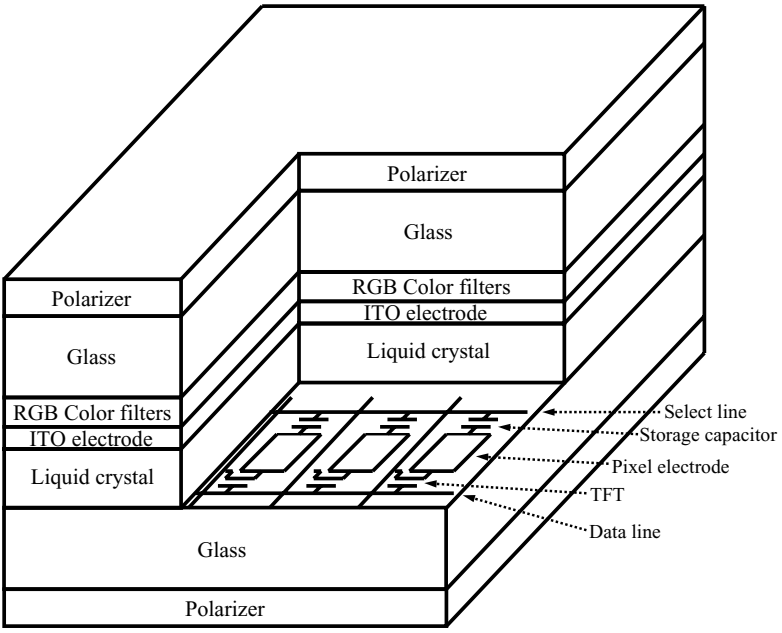

Fig. 6.7. Cut-away view of an active-matrix liquid-crystal display.

An AMLCD is a non-emissive display in which the transmission of light through a picture element, i.e., a pixel, is controlled by application of a voltage across a capacitor, which consists of a liquid crystal dielectric and two transparent conductive electrodes on glass substrates. The applied voltage changes the relative alignment of the anisotropic liquid crystal which, in turn, changes the state of polarization of light being transmitted through a given pixel.

Figure 6.7 provides a slightly more detailed look at the basic operating principles of an AMLCD. Assuming that light enters through the bottom from a backlight source, the combined effect of the top & bottom polarizers and the variable state of polarization obtained by application of a voltage across the liquid crystal capacitor determines the extent of light transmission through a given pixel. As indicated in Fig. 6.7, red, green, and blue filters are used in a sub-pixel cluster to realize a full-color display.

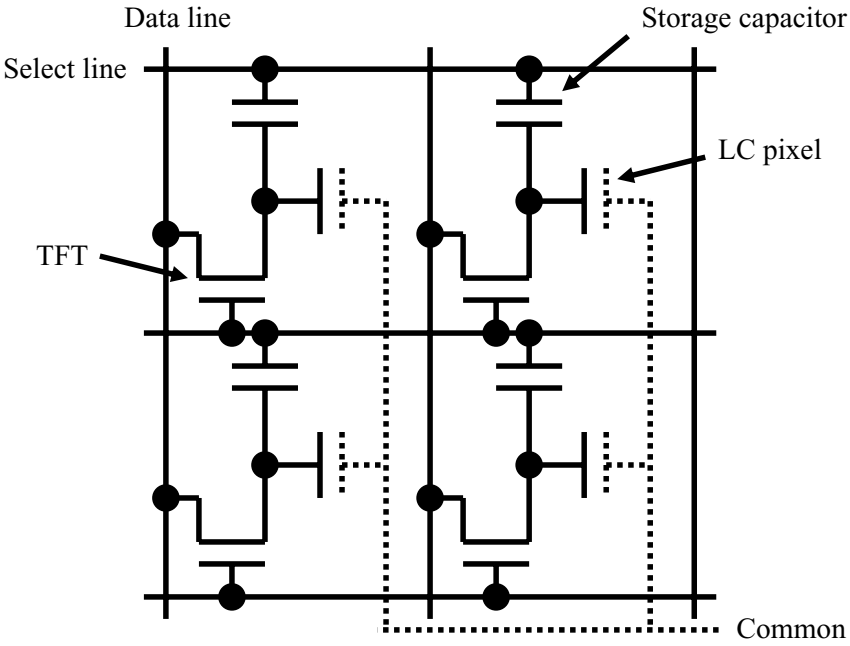

Fig. 6.8. Equivalent circuit representation of four pixels in an active-matrix liquid-crystal display.

A simple equivalent circuit representation of the active-matrix portion of an AMLCD is shown in the upper side of the bottom glass of Fig. 6.7, and also in Fig. 6.8. The idea behind active-matrix addressing is to use a transistor for pixel selection and voltage control to that pixel. The use of a transistor switch in an active-matrix scheme should be distinguished from the simpler case of passive-matrix addressing in which pixels are defined by the intersection between mutually orthogonal conducting lines. The simplicity of passive-matrix addressing, however, is obtained at a cost of much poorer performance (e.g., gray scale, contrast ratio, resolution, image quality, etc.), especially as the display size increases.

Returning to Fig. 6.8, consider AMLCD operation from an active-matrix addressing perspective. The display is addressed one line at a time. A row is selected by application of a row voltage via the select line, thereby turning on all of the TFTs whose gates are connected to this row. While a given row is selected, the relative transmission of light through a specific pixel is established by the magnitude of its corresponding column voltage applied via its data line. Application of this column voltage charges the LC capacitor and also a storage capacitor, which supplements the charge storage capability of a pixel. After a row has been addressed, it is deselected by reducing the row voltage. Pixels in the deselected row maintain their programmed relative transmission until the next addressing cycle, at least to the extent that charge remains on the LC and storage capacitors. Each row in the display is sequentially addressed once every frame period.

Given this minimal AMLCD background, the transparent electronics application opportunity of interest is to employ a TTFT as a transparent switch in an AMLCD pixel. Typically, amorphous silicon (a-Si) TFTs are used for this purpose. TTFTs offer several advantages compared to a-Si TFTs. First, a TTFT is transparent, which, in principle, could obviate the need for light-shielding, as required in current state-of-the art AMLCDs since a-Si is a photoconductor. Second, the mobility of a-Si TFTs is ~1 $cm^2V^{-1}s^{-1}$, considerably less than that reported for many different types of TTFT. A higher mobility translates into more current drive, which leads to improved charging of the LC and storage capacitor. Third, the a-Si TFT turn-on voltage is typically negative (den Boer 2005), whereas some TTFTs have been demonstrated to possess small, positive turn-on voltage, which is better suited to AMLCD applications. Fourth, TTFTs are less complicated devices to fabricate, primarily because source and drain contacts may be applied directly to the channel layer, eliminating the need to separately dope the channel. Fifth, early-stage bias-stress stability research suggests that a mature TTFT technology will employ devices with better long-term aging properties than is available with a-Si TFT technology. Sixth, TTFTs are simpler to fabricate, not requiring doping of the region underneath the source-drain contact, nor toxic process gases such as silane.

Even with these TTFT advantages, it is unlikely that TTFTs will soon displace a-Si TFTs in mainstream AMLCD applications. The primary reason for this is that a-Si TFTs constitute an adequate and proven technology which is industrially well established and which benefits from immense capital investment over an extended period of time. Thus, it is unlikely that the apparent performance advantages of TTFTs noted above will lead to large-scale commercial AMLCD implementation in the near future.

Moreover, there are several hurdles that a TTFT must overcome before they could be considered to be a viable contender for this AMLCD switching transistor application. These include low-temperature (less than ~300 ºC) processability, verified long-term stability, and proven high-volume manufacturability.

This pessimistic prediction re the near-term use of TTFTs in AMLCDs underscores the importance of the 'technological immaturity' TTFT demerit included in Table 3.1. Note that this is the only weakness included in Table 3.1 which applies, since an AMLCD transparent switch application involves *local* rather than *global* transparency, so that high resistance is not relevant. Additionally, this application involves low frequency operation and is not hindered by the unavailability of complementary p-type devices.

6.3.5 AMOLED backplane

In certain respects, the active-matrix organic light-emitting device (AMOLED) backplane application is similar to that of the AMLCD application just discussed. This is the case because active-matrix addressing is again employed in order to achieve identical display performance advantages as previously reviewed, i.e., larger display dimensions and improved gray scale, contrast ratio, resolution, image quality, etc.

However, there are some important differences between AMLCD and AMOLED applications. First, an LCD is a non-emissive display which, it turns out, requires the use of a transistor to provide *voltage control* in order to accomplish active-matrix addressing. In contrast, an AMOLED is an emissive device which, it turns out, necessitates the use of *current control* to set the brightness of a pixel. As evident from the following discussion, active matrix current control is more difficult to accomplish, requiring the use of more than one transistor per pixel. Additionally, current control places more severe constraints upon pixel transistors in terms of long-term stability and device uniformity with respect to threshold voltage amd channel mobility.

A second important difference between an AMLCD compared to an AMOLED application, particularly in the context of transparent electronics, is the lack of maturity of the AMOLED display industry. Since

AMOLED displays are just now beginning to enter the market, we contend that a TTFT backplane may be a viable option, in dramatic contradistinction to the relatively mature nature of the AMLCD industry in which it is exceedingly difficult to displace a-Si TFTs in active matrix switching transistor applications.

The emissive nature of an OLED compared to the non-emissive nature of a LCD is noteworthy since it results in a display which has a faster response time, a wider viewing angle, higher contrast, consumes less power, is lighter weight, and is better suited to flexible substrate applications (Kuo 2004a,b; den Boer 2005). Present day critical OLED technology challenges involve reliability/lifetime, manufacturability, and cost.

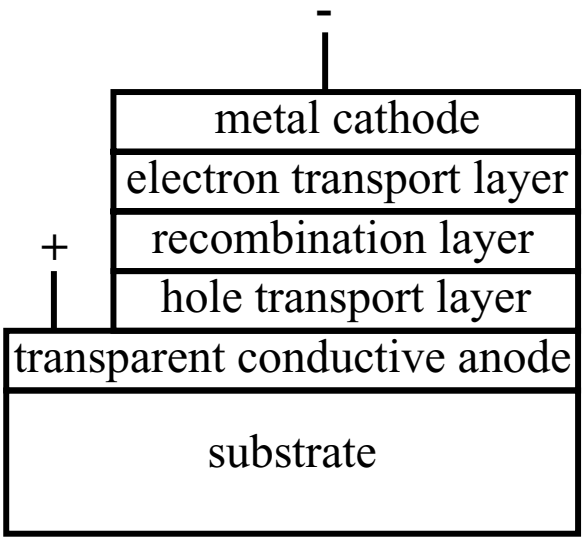

Fig. 6.9. Basic structure of an organic light-emitting device (OLED).

Figure 6.9 illustrates the basic structure of a generic OLED (Shinar 2004; Kafafi 2005). Although three organic layers - electron transport, recombination, and hole transport - are indicated in Fig. 6.9, an actual OLED may have more layers than this, or alternatively as few as a single organic/polymer layer. The essential operation of an OLED relies on the injection and transport of electrons and holes from contact electrodes into an intermediate region, where radiative recombination occurs, giving rise to the emission of light. An OLED is operated using a DC voltage, and possesses rectifying current-voltage and brightness-voltage characteristics. When the voltage polarity as specified in Fig. 6.9 is applied, the OLED is

forward biased so that appreciable current flows. The magnitude of current flow through an OLED is proportional to its brightness.

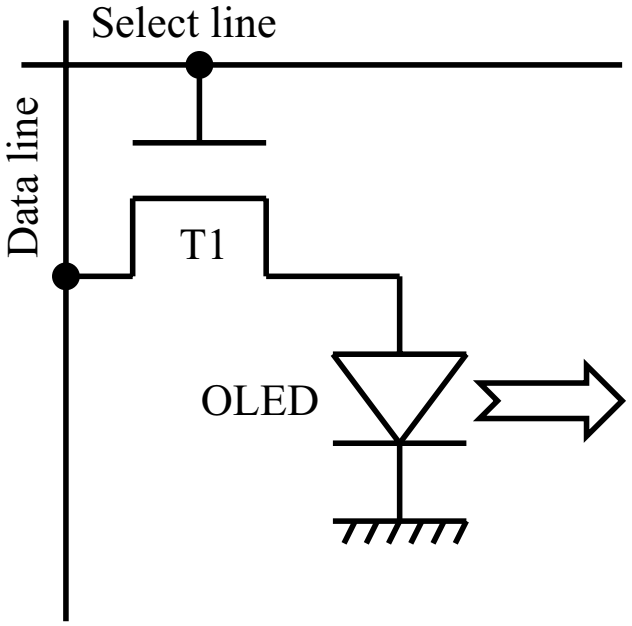

Fig**. 6.10.** An active-matrix organic light-emitting device (AMOLED) pixel addressing scheme employing one n-channel transistor.

Figure 6.10 indicates what AMOLED addressing would look like if a pixel employed only a single transistor, as is the case for an AMLCD (Wu et al. 1996; Stewart et al. 1998). Integration of an OLED with a single transistor driver is sometimes referred to as an 'organic smart pixel' (Dodabalapur et al. 1998). A single transistor scheme is the simplest active matrix addressing strategy to implement, and thus provides the highest manufacturing yield. As is the case for an AMLCD, an AMOLED display is addressed one line at a time. Therefore, in a single transistor AMOLED addressing scheme, each pixel emits light only when its row is being addressed. Thus, an OLED is on only for a small fraction of the frame period, 1/N, where N is the number of display rows. This means that a light source must be driven harder in order for it to emit the equivalent amount of light in a fraction of the frame period compared to what it would emit if the pixel is designed so that the light source emits continuously during the entire frame period. Operation of a display at an elevated drive current will adversely affect the display lifetime. For these reasons, the one tran-

sistor, 'smart pixel' active-matrix addressing scheme shown in Fig. 6.10 is impractical.

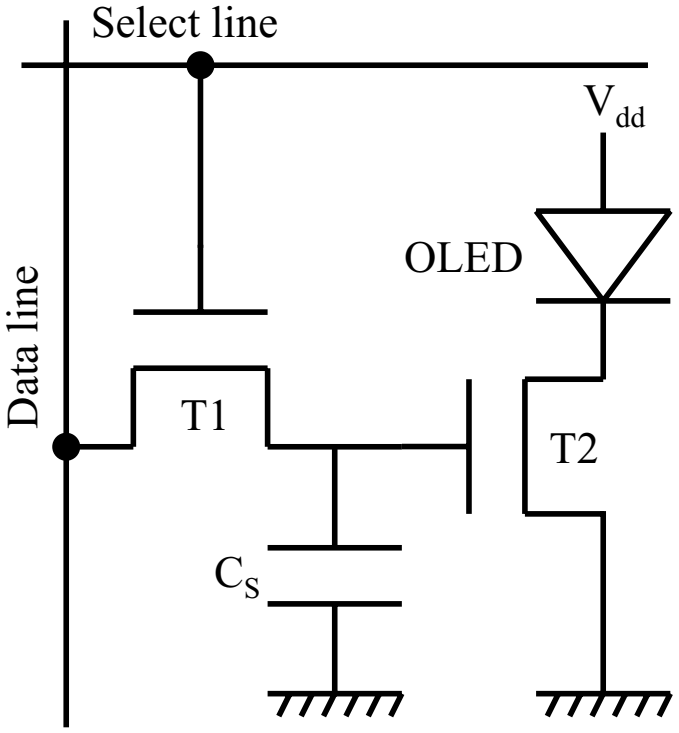

Fig. 6.11. An active-matrix organic light-emitting device (AMOLED) pixel addressing scheme employing two n-channel transistors and one capacitor.

A two transistor pixel addressing scheme, such as the one shown in Fig. 6.11, is a distinct improvement over the single transistor pixel approach given in Fig. 6.10. This pixel consists of a control or select transistor (T1), a drive or current source transistor (T2), and also a storage capacitor (C_S). Pixel operation is as follows. This display is again addressed one row at a time. During addressing, a row is selected by driving the row voltage (select line) high, thus turning on T1. While a row is selected, the desired brightness of the pixel selected is programmed by choosing its corresponding column (data line) voltage magnitude. A larger data line voltage will drive more current into the pixel, thereby charging C_S up to a larger voltage. At the end of the addressing period, the row is deselected by letting the select line voltage go low, turning off T1, and thereby isolating the pixel from the data and select addressing lines. During the remainder of the frame period, until the next addressing cycle for this row, the voltage

across C_S keeps T2 turned on to the extent it was programmed during addressing, thus controlling the amount of current flowing through the OLED, and hence its brightness. T2 operates as a current source, maintaining a constant current to the OLED, at least to the extent that the voltage across C_S, and hence the transistor gate-source voltage V_{GS}, remains constant. Note that the OLED is placed on the drain side of T2, instead of on its source side. This is OLED placement is intended to disencumber the current source performance of T2 from OLED degradation. That is, if the OLED is placed on the source side of T2 and if the threshold voltage of the OLED changes with time due to degradation, the magnitude of the current flowing through T2 would change, since V_{GS} would change. Finally, notice that there are three lines entering each pixel, i.e., the data line, the select line, and the power supply line, V_{dd}.

The two transistor AMOLED addressing scheme presented in Fig. 6.11 is superior to the one transistor scheme indicated in Fig. 6.10 since the addition of a second transistor and of C_S provide memory and control which enables the pixel to remain on for the full duration of the frame period. However, there are several liabilities inherent in this two-transistor design. First, the current supplied by the driver current source T2 depends upon the transistor threshold voltage and channel mobility. If either or both of these vary as a function of temperature or operating lifetime, the current supplied to the OLED will change. Second, a threshold voltage and/or a mobility nonuniformity across the display will lead to a corresponding brightness nonuniformity. Third, degradation of the OLED with time results in decreasing brightness and/or brightness nonuniformity, depending on whether the degradation is absolute, in a global sense, or is differential in nature. These considerations mandate the use of circuit-based pixel compensation techniques in practical AMOLED displays.

The design of AMOLED circuit architectures employing compensation is a topic of considerable current interest (Dawson et al. 1998; Aaerts et al. 2002; Fish et al. 2002; Sakariya et al. 2004; Church and Nathan 2005; Kuo 2004a; Nathan et al. 2005; Troccoli et al. 2005). Although three-transistor solutions have been proposed (Fish et al, 2002; Ashtiani et al. 2005; Troccoli et al. 2005), most pixel architectures employ four transistors. AMOLED pixel compensation strategies usually involve voltage and/or current programming. For a detailed overview of AMOLED circuit architecture considerations, the reader is advised to consult Nathan et al. 2005, Troccoli et al. 2005, and references therein.

Figure 6.12 is an example of a promising four transistor AMOLED pixel architecture which, for our purposes, illustrates some of the basic design and operational features of interest to transparent electronics (Sakariya et al. 2004; Church and Nathan 2005; Nathan et al. 2005).

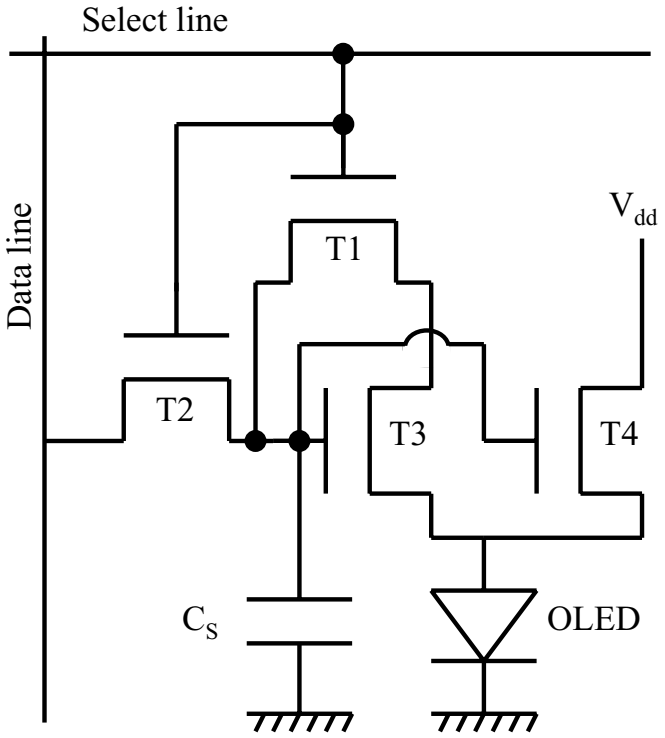

Fig. 6.12. An active-matrix organic light-emitting device (AMOLED) pixel addressing scheme employing four n-channel transistors and one capacitor.

Consider the operation of the circuit shown in Fig. 6.12. Addressing is once again accomplished in a line-by-line manner. A line is selected by forcing the select line high, thereby turning on both T1 and T2. Immediately after the line is selected, current flows through T2, charging up C_S. As the voltage across C_S rises, T3 begins to turn on so that current also flows through T1 and T3 to ground through the OLED. The voltage across C_S stabilizes when all of the current flows through T1 and T3, and none through T2. Note that this programming of voltage across C_S does not depend on the T3 and T4 threshold voltages.

Once a line has been addressed and the voltage across C_S has been programmed, the select line is driven low, thereby turning off T1 and T2, iso-

lating the row from the select and data lines. To understand how the circuit shown in Fig. 6.12 works, it is best now to change perspective and to recognize that when the voltage across C_S during addressing reaches a steady-state, that this equivalently corresponds to a situation in which the current through T3 has been programmed. This current addressing perspective is useful once it is recognized that T3 and T4 constitute a current mirror, in which the steady-state current flowing through T3 at the end of the addressing period can be effectively copied and mirrored through T4 during the remainder of the frame period after addressing when T3 turns off concomitantly with T1. This current mirroring from T3 to T4 is accomplished by having C_S in common with both of their gates. A current mirror architecture is attractive for pixel compensation since it is independent of the threshold voltages of the transistors comprising the current mirror. (Sakariya et al. 2004; Nathan et al. 2005)

What does this AMOLED pixel architecture discussion have to do with transparent electronics? Currently, two options are being considered for AMOLED backplanes: a-Si and low-temperature polysilicon. It is our contention that transparent electronics-based AOSs constitute a very attractive alternative technology for this application. Table 6.2 is a comparison between these three technologies.

Table 6.2. A comparison between a-Si, low-temperature polycrystalline silicon, and transparent electronics technologies for AMOLED display backplane applications.

Property	Amorphous silicon (a-Si)	Polycrystalline silicon	Transparent electronics
Manufacturability, infrastructure	mature, proven	emerging	early stage R&D
Grain size	amorphous	0.5-5 μm	amorphous
Threshold voltage uniformity	good	fair	?
Threshold voltage stability	poor	good	good
Mobility	<1	100-500	~10-30
Mobility uniformity	good	fair	?
Device type	NMOS	CMOS	NMOS
Transparency	opaque, light-sensitive	opaque, light-sensitive	transparent

From a risk perspective, a-Si is the clear technology of choice for AMOLED backplane applications because of its preponderance in current-

art AMLCDs. It is a mature, proven, manufacturable technology which is well established in the commercial sector, having an existing infrastructure which is readily accessible and scalable to meet the projected needs of a future AMOLED technology. However, a-Si technology has two potential Achille's heels with regard to near-term and future AMOLED display applications, poor stability and channel mobility/current drive, as discussed in the following two paragraphs. Note that we assert these two limitations to be inherent in this technology, and very likely to be 'unfixable', given the nature of these problems and the mature state of a-Si TFT technology.

First, the threshold voltage stability of a-Si TFTs is poor (Lih et al. 2004; Troccoli et al. 2005). As discussed further in Section 5.3.3, we believe this stability to be a fundamental attribute of a-Si TFTs (Powell et al. 1992; van Berkel 1992; Powell et al. 1993; Powell et al. 1996; Powell et al. 2002). This instability appears primarily to be a consequence of the metastable nature of a-Si itself. However, it is also associated with the metastability of the silicon nitride gate dielectric. Silicon nitride is used because is its metastability opposes and partially cancels that of a-Si. We concur with the assertion that these inherently unstable a-Si TFTs are actually well suited to the relatively non-demanding AMLCD pixel application in which TFTs are used for *voltage control* in a simple switching context. However, we contend that the stability of a-Si TFTs is inadequate for the more challenging *current control* application associated with an AMOLED display.

Second, the mobility, and hence the current drive of a-Si TFTs is poor. It is possible that clever pixel circuit design strategies and improvements in OLED efficiency will suffice for AMOLED backplane display applications for a generation or two. However, we think that sooner or later the poor current drive capability of a-Si TFTs will be insufficient. Moreover, future applications will likely require the integration of drive electronics onto the display substrate. It will be exceedingly difficult to accomplish this using a-Si technology.

Low-temperature polysilicon technology is an appealing alternative to a-Si TFTs for AMOLED backplane applications in several respects. First, polysilicon TFTs are stable and have much better channel mobility / current drive than a-Si TFTs. Moreover, CMOS is available with polysilicon technology while a-Si TFTs are only NMOS. These considerations make polysilicon technology very attractive for future AMOLED displays since high drive current and CMOS are ideal for integrating drive electronics onto the display substrate.

Nonetheless, polysilicon technology has certain demerits of its own with respect to AMOLED backplane applications (Jang 2004; Church and Nathan 2005). Currently the most debilitating problem appears to be associated with its manufacturability, i.e., obtaining adequate yield and uniformity across the display. The silicon re-crystallization process is apparently particularly challenging. Other concerns involve the increased process complexity (e.g., an increase in the number of masks), higher cost, worldwide polysilicon capacity, as well as threshold voltage and mobility uniformity, as noted in Table 6.2.

Inclusion of transparent electronics in Table 6.2 as an AMOLED backplane option is meant to be intentionally provocative. Although transparent electronics is extremely new compared to a-Si and polysilicon technologies, we believe that it is not at this time premature to consider it as a possible competitor, even for a high-stakes application such as this one. With respect to channel mobility, transparent electronics holds an intermediate position between a-Si and polysilicon technologies. The channel mobility of TTFTs is high enough to possibly allow for integration of drive electronics onto the display substrate. However, transparent electronics involves exclusively NMOS technology, at least at this time, which is not as attractive as CMOS for integrated driver applications.

The two question marks included in column three of Table 6.2 and a comment regarding stability are of crucial importance for establishing the manufacturability and near-term commercial potential of transparent electronics. As discussed in Section 5.3.3, our recent transparent electronics stability work suggests that a mature glass-substrate-based transparent electronics technology will offer TFTs that are more stable than a-Si TFTs. Thus, we are optimistic in this regard. However, more work is required to ascertain whether threshold voltage and channel mobility uniformity challenges can be met in transparent electronics. This work will involve scaling towards high-volume manufacturability.

The last row of Table 6.2 reminds us that the truly unique aspect of transparent electronics is visible transparency. We believe that this aspect of transparent electronics may be a key and crucial consideration for AMOLED display applications. The use of TTFTs, a transparent capacitor, and transparent local interconnects could significantly increase the aperture ratio of an AMOLED pixel, i.e., the fraction of the pixel from which light can be emitted. Since TTFTs do not require light shielding, unlike a-Si and polysilicon TFTs, more of the pixel real estate is available for TTFT

placement so that TTFT dimensions, and hence current drive, may be greater for a transparent electronics pixel. The only opaque portion of the pixel would be the global metal select and data lines; everything else could, in principle, be transparent. Thus, this AMOLED backplane application requires local rather than global transparency. AMOLED integration with transparent electronics would be compatible with a conventional, metal cathode-on-top OLED structure, as sketched in Fig. 6.9. Another attractive feature of TTFTs is their simplicity of processing due to the fact that source/drain contacts may be directly placed onto the channel substrate, so that additional steps associated with source/drain doping are obviated.

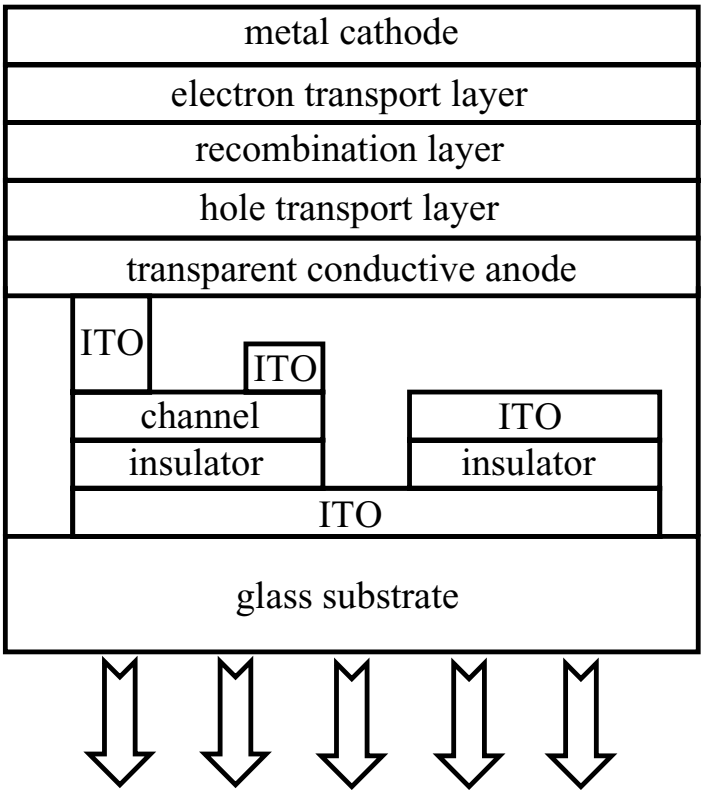

Fig. 6.13. Integration of a bottom-emitting organic light-emitting device (OLED) with a locally-transparent, active-matrix pixel. The five top layers constitute the OLED. Only two components of the active-matrix pixel are indicated, a bottom-gate TTFT (left) and a storage capacitor (right). ITO denotes indium tin oxide, a transparent conductor which is employed as a TTFT gate, source, and drain electrode; capacitor electrode, and a local interconnect between the TTFT & the OLED and also between the TTFT and the storage capacitor.

6.3.6 Transparent charge-coupled devices (CCDs)

Consider the operation of a conventional, silicon-based charge-coupled device (CCD) from the perspective of a shift register, as shown in Fig. 6.14a. The purpose of a shift register is to transfer digital information, i.e., a 1 or 0, down a line of gates. The key semiconductor device giving rise to CCD functionality is a metal-oxide-semiconductor (MOS) capacitor. The shift register indicated in Fig. 6.14a possesses eight MOS capacitors, as defined by black 'metal' (or an alternative material, such as doped polysili con) electrodes sitting on an insulator (usually silicon dioxide for silicon-

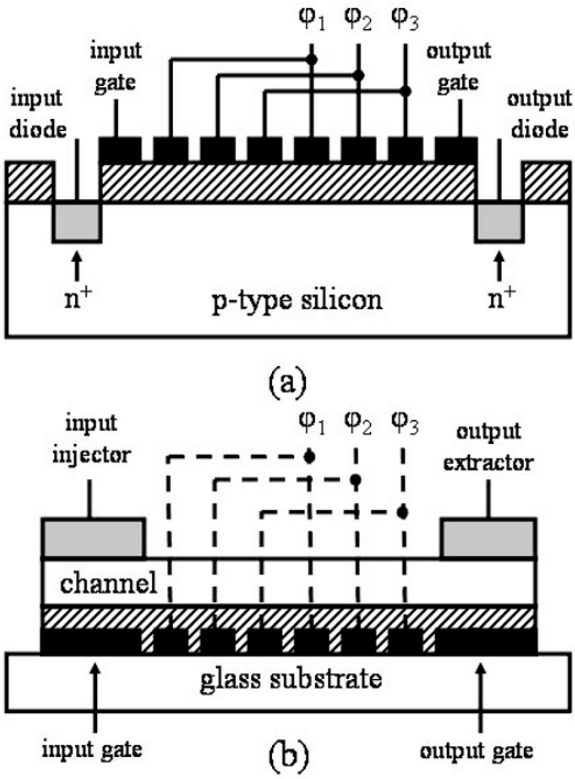

Fig. 6.14. Charge-coupled device (CCD) prototypes. (a) A conventional silicon-based three-phase, two-bit, n-channel, *inversion*-mode shift register. (b) A transparent electronics-inspired three-phase, two-bit, n-channel, *accumulation*-mode shift register.

based CCDs) which is in turn sitting upon a p-type silicon substrate. Each MOS capacitor is capable of forming an *inversion* layer at the silicon-insulator interface, if a sufficiently large voltage of proper polarity (positive for the case under discussion) is applied to the metal gate electrode. This inversion layer consists of minority carrier electrons for the Fig. 6.14a case with a p-type substrate; thus it is denoted as an *n-channel*. Charge transfer between gates can be accomplished if a sequence of appropriate time-varying voltages is applied to neighboring electrodes so that the potential seen by inversion layer electrons attracts electrons down the channel. φ_1, φ_2, and φ_3 represent three clocked, time-varying voltage pulse waveforms which facilitate charge transfer along the channel, giving rise to so-called *three-phase* operation. Two bits of information may be processed along the channel indicated in Fig. 6.14a, since two sets of phased MOS capacitors are available to transfer, or to not transfer inversion layer electrons. Charge injection and extraction to and from the CCD transfer gate array is accomplished using the input and output diodes/gates, respectively. These input and output diodes are fabricated by the creation of heavily doped n^+ regions in the p-type silicon substrate. Note that the silicon-based CCD shift register shown in Fig. 6.14a can be alternatively viewed as a multi-gate MOSFET in which the input and output diodes serve as the source and drain diffusions, respectively. A more detailed treatment of CCD operation, device structures, applications, etc. is available in several more comprehensive references (Hobson 1978; Howes and Morgan 1979; Beynon and Lamb 1980; Theuwissen (1995); Reike 2003; Sze and Ng 2007).

A transparent electronics-inspired CCD shift register is given in Fig. 6.14b, and is analogous to the silicon-based CCD shift register shown in Fig. 6.14a. This device has six MOS capacitors connected to three phases, resulting in two bits of information transfer. However, note that the gate electrodes are now located on a glass substrate at the bottom of the device, and the MOS capacitor consists of a transparent 'metal' (most likely ITO), and insulator (not necessarily silicon dioxide), and a channel layer (which would be chosen from one of the TTFT channel materials). The input and output gate dimensions are drawn to be a different size than that of the transfer gates in order to underscore that these input and output gate electrodes are used for the injection and extraction of electrons into or out of a gate-voltage-induced channel at the channel layer/insulator interface. The input and output gate, as well as the input and output extractor would likely be fabricated using ITO. A fundamental difference between the transparent CCD shift register of Fig. 6.14b compared to the silicon-based CCD shift register indicated in Fig. 6.14a is that the transparent CCD

channel is an n-type *accumulation layer* rather than an n-type *inversion layer*. Additionally, no input and output gate diffusion is required for the transparent CCD since the off-current of this device is mediated by the extremely large resistance of the channel layer, rather than the back-to-back diodes required in the silicon-based realization. Recognize that the transparent CCD shift register sketched in Fig. 6.14b can be alternatively perceived to be a multi-gate TTFT in which the input and output injectors constitute, respectively, the source and drain electrodes.

Before discussing possible transparent-CCD applications, it is appropriate to recognize and address a potential liability of the CCD structures sketched in Fig. 6.14. For efficient charge transfer between CCD transfer gates, it is essential that the potential wells underneath neighboring MOS capacitors overlap. This requires having close physical separation between adjacent MOS capacitors. It appears that more physical separation is allowable in a silicon-based CCD, since depletion layer dimensions may be rather large (up to ~1 μm) so that significant lateral electrostatic coupling is possible through the bulk silicon substrate, compared to a transparent CCD, in which electrostatic coupling occurs via a very thin channel layer, whose thickness would be ~10-80 nm.

A multiplicity of solutions to this 'narrow-gap' CCD problem have been proposed and implemented in silicon-based CCD technology (Howes and Morgan 1979; Beynon and Lamb 1980). One simplified approach for improving charge transfer via overlap between transfer gates is shown in Fig. 6.15a. In this approach, gate overlap is achieved through the use of two gate 'metals', one buried within the gate dielectric and the other sitting upon the top surface of the gate insulator. Although a significant motivation for the dual-gate structure of Fig. 6.15a involves the realization of two-phase operation due to the formation of an asymmetric potential well when a surface and buried gate are electrically tied together (Howes and Morgan 1979), the essential message of Fig. 6.15 with regard to our present discussion is that use of gate overlap is a means for overcoming the 'narrow-gap' CCD charge transfer problem.

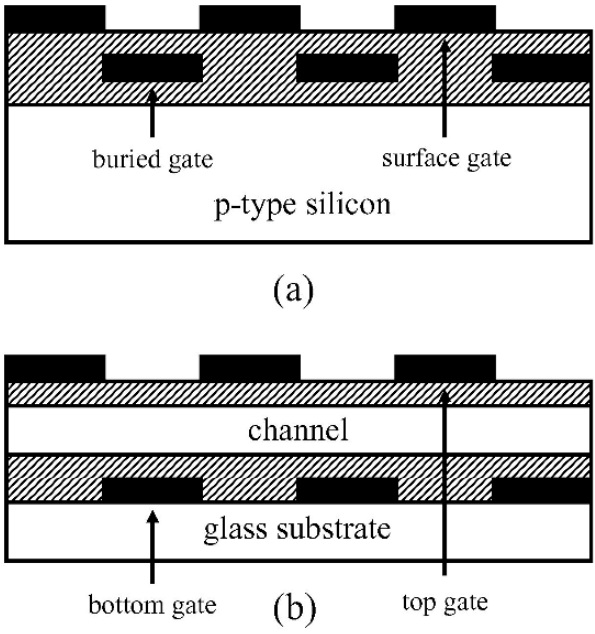

Fig. 6.15. Dual-gate charge-coupled device (CCD) structures, illustrating simplified approaches for improving charge transfer via gate overlap. (a) A conventional silicon-based n-channel, *inversion*-mode CCD. (b) A transparent electronics-inspired n-channel, *accumulation*-mode CCD.

With this in mind, consider the transparent-electronics-inspired dual-gate CCD structure indicated in Fig. 6.15b. Essentially, such a CCD would correspond to a multi-double-gate TTFT in which the source-gate and drain-gate contacts (not shown in Fig. 6.15b) would serve, respectively, as the CCD injector and extractor. Operation of the transparent CCD of Fig. 6.15b would involve alternating charge transfer between the top and bottom insulator-channel interfaces. The performance of such a device, in terms of charge transfer efficiency, etc., is not known, since at

this time such a transparent CCD is a only device concept, which has not yet been reduced to practice.

Silicon-based CCDs are primarily used in image sensor and shift register applications. Likewise, a transparent CCD would probably also be most attractive for these applications. For imaging applications, the photoconductive properties of the TTFT channel material must be considered, as briefly discussed in Section 3.3. CCD transparent shift registers could find application, for example, in on-glass row driver applications for AMLCDs (den Boer 2005). In addition to imaging and shift register applications, the performance and manufacturability of transparent CCDs, when reduced to practice, compared to TTFT-based circuits will determine whether other digital or analog electronics or signal processing applications emerge for transparent CCDs.

6.4 Barely scratching the surface

Composing a chapter on transparent circuits makes you feel as if you are writing science fiction. There's so little to write about, in terms of what has been reported on this topic to date, that you feel like you just have to make it up! However, circuits are where the rubber meets the road for most commercial applications. Thus, it is an extremely important topic and **much** more work needs to be done. This is an area ripe for innovation.

7 The Path Forward

7.1 Where do we go from here?

A transparent electronics *technology identification* roadmap is offered in Table 7.1. The main intent of this roadmap is to categorize some of the work that is perceived to be of primary significance for fostering the rapid development of transparent electronics. Five basic tasks are included, each of which is briefly discussed in the following.

Table 7.1. A transparent electronics technology identification roadmap.

Task	Objective
TTFT improvement	TTFT quality will define the application space
TTFT stability assessment & optimization	establish application space
circuit design & fabrication	establish application space
new technology identification (non-TTFT)	novel, disruptive applications?
application proof-of-concept	demonstrate & validate technology

- TTFT improvement. As discussed in Chapters 2 and 5, a TTFT is ***the*** critical device, foundational to transparent electronics. Thus, the performance quality of this device dictates, to a large extent, the range of possible transparent electronics applications. The essential TTFT performance figures-of-merit are the turn-on voltage polarity and magnitude (V_{ON}), the channel mobility as a function of gate voltage [$\mu(V_{GS})$], and the subthreshold swing (S). Any material or process modification which leads to a small and positive V_{ON}, a larger μ with an abrupt and saturated V_{GS}-V_{ON} overvoltage transition, and/or a smaller S is highly desirable. Additionally, the run-to-run and across-the-substrate uniformity of V_{ON}, $\mu(V_{GS})$, and S are crucially important for most applications.

- TTFT stability. In addition to basic electrical performance, TTFT stability is also vital for establishing the suitability of this technology to a given application. As presented in Section 5.3.3, early TTFT stability results are quite encouraging. However, more work is required to assess and optimize TTFT stability. Better TTFT stability implies a broader range of commercial applications.

- Circuit design and fabrication. As considered in Chapter 6, very few transparent-electronics-based circuits have been designed, simulated, built, and tested. Additionally, as argued in Chapter 2, it is not yet clear which circuit families or topologies are best-suited to transparent electronics. In order to establish its potential value, many different types of transparent electronics circuits should be explored. In this vein, Table 7.2 is offered as an initial starting point for exploratory development of digital, analog, and power electronics technologies within the overall transparent electronics umbrella.

Table 7.2. Toolboxes for the exploratory development of three possible transparent electronics circuit families (Mayaram 2006).

Digital toolbox	Analog toolbox	Power toolbox
NAND gate	common-source amplifier	AC-DC converter
multiplexer	differential amplifier	DC-DC converter
static D-flip flop	current mirror	DC-AC converter
frequency divider	2-stage operational amplifier	

- New technology identification (non-TTFT-based). The point here is to look for novel and perhaps disruptive non-TTFT-based technologies, and to undertake this at a very early stage of development. Transparent electronics is so new that very little `blue-sky' thinking has been committed to this topic. A transparent CCD is an example of new technology identification. Obviously, once a new technology has been identified, it should be assessed and developed, if warranted.

- Application proof-of-concept. A new device, circuit, or system concept may appear quite attractive prior to its reduction-to-practice. However, since there are a semi-infinite number of `show-stoppers' which can render a prospective technology commercially dead-on-arrival, it is best to accomplish a series of demonstration proof-of-concepts in order to help validate the viability of a new idea. The sooner this is accomplished, the better.

Narrowing the focus of discussion to that of TTFTs, a TTFT *technology development* roadmap is included as Table 7.3. The purpose of this table is to enumerate specific tasks which require further attention in order to accelerate transparent electronics development toward commercialization. These topics are briefly amplified in the following.

Table 7.3. A TTFT technology development roadmap.

Task	Objective
high-k gate insulators	improve TTFT performance
channel layer improvement	improve TTFT performance (e.g., V_{ON}, channel mobility)
channel layer passivation	required for device integration
new channel layer exploratory development	improve TTFT performance, reliability, manufacturability
new devices	improve frequency performance
p-TTFT development	realize a c-TTFT technology
low-temperature process optimization	plastic substrate compatibility
low-cost processing	increase application space

- High-k gate insulators. As discussed in Section 5.3, increasing the gate capacitance of a TTFT increases its current drive and, as illustrated in Fig. 5.13, can significantly improve its subthreshold swing, S. This dramatically improves its device and circuit performance. This improvement comes at a cost, however, since the parasitic overlap capacitance of the TTFT also increases, which is undesirable. Thus, self-aligned gate strategies should be investigated concurrently with the development of high-k gate dielectrics in order to minimize parasitic capacitance.

- Channel layer improvement. As discussed previously in this section under the TTFT improvement category, TTFT performance improvments may to a large extent be ascribed to improvements in V_{ON}, $\mu(V_{GS})$, S, and stability. Once a channel layer has been selected, channel layer improvement may possibly be accomplished by modification of the channel layer thickness, deposition parameters, post-deposition processing treatments, the starting material purity, or channel layer co-doping strategies. Very little work has been performed to date with respect to this type of channel layer optimization.

- Channel layer passivation. Channel layer passivation is briefly considered in Sections 2.2.3 and 6.2.2. Passivation is a crucially important issue since the realization of more complex transparent

integrated circuits depends on successful integration of interlevel dielectrics and interconnects. Much more work is required in this regard.

- New channel layer exploratory development. As discussed in Chapters 2 and 4, we advocate the use of amorphous oxide semiconductors (AOSs) as appropriate channel layers for TTFT applications. As identified by Hosono et al., there are a total of 108 AOS ternary combinations (e.g., $ZnSnO_3$), of which we would reduce this to 28 if certain toxic and costly cations are eliminated from consideration; explicitly, this leaves the following cations for consideration: Cu, Zn, Ga, Ge, In, Sn, Sb, and Bi (Hosono et al. 1996b). Additionally, there are 56 AOS restricted quaternary combinations (e.g., $ZnInGaO_4$). In reality, there are many more possibilities than those just specified since each combination has a variable cation ratio (e.g., $ZnSnO_3$, Zn_2SnO_4, $ZnSn_2O_5$, $Zn_{2.5}SnO_{4.5}$, etc.). Most of these AOS materials systems are unexplored. How many of them would function as high-performance TTFT channel materials? Which ones are optimal? Much more exploratory development is required before these questions can be answered.

- New devices. As overviewed in Section 5.4, several types of alternative transistors are identified as potentially useful for transparent electronics applications. These include static-induction transistors (SITs), vertical TFTs, several types of hot electron transistors, and nanowire transistors. The primary impetus for considering these novel device types is to improve the high-frequency performance of transparent electronics. Investigation of the devices specified herein, as well as other types of devices not mentioned, could lead to an expansion of the transparent electronics application space.

- p-TTFT development. A complementary TTFT technology, c-TTFT, in which both n-channel and p-channel TTFTs are available is highly desirable, for all of the reasons mentioned in Section 3.2. However, as attractive as c-TTFT technology is, at this time it appears to be a very elusive goal, as discussed in Section 5.3.4.2. Nevertheless, even though it is a difficult task, we believe that research and development efforts devoted to the realization of a p-TTFT are justified since the payoff is so great.

- Low-temperature process optimization. Many emerging electronics applications, e.g., flexible electronics, require the use of plastic substrates, which in turn restrict the maximum processing temperature to less than ~150-300 ºC, depending on the specific substrate employed. It is almost always easier to prepare a high-quality inorganic thin film at a higher processing temperature. Thus, it is challenging to fabricate high-performance and stable TTFTs and other transparent electronics devices at processing temperatures as low as required for plastic substrate applications. More effort is required to accomplish this goal. In our experience, the lower the process temperature, the more difficult the task.

- Low-cost processing. Cost is a primary consideration in many emerging electronics technologies, such as disposable and wearable electronics. It is likely that some of these applications will require the use of ultra-low-cost manufacturing methods such as printing and stamping, instead of more conventional, higher cost electronics processes involving physical or chemical vapor deposition. In our experience, AOS channel layers are well-suited to such applications, although more research and development work is necessary before these technologies are mature enough for commercialization.

As a final parting shot, please recognize that although we have strived in this monograph to focus most of our attention on ***transparent*** electronics, it is our strong conviction that much of what we have discussed herein applies equally well to new, emerging technologies such as macroelectronics or flexible, large-area, low-cost, disposable, and wearable electronics. In these fields of developmental activity, the limits are also difficult to see - even if the constituent devices are not transparent!